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# MACHINE LANGUAGE 

## PROGRAMMING

## MADE SIMPLE FOR YOUR

SINCLAIR $2 \times 80 \& 2 \times 81$

Melbourne House Publishers

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## AROUND

MACHINE LANGUAGE


This book is designed to be an introduction the field of machine and assembly language programming for the Sinclair $2 \times 80$ and $2 \times 81$.

It may be that you are coming to this book with no clear idea of what machine language programming is all about. Indeed the difference between machine language and assembly language may not be clear to you, nor indeed how they differ from programming in BASIC.

So let us look at the way a computer operates:


What this diagram shows is that there is a barrier between the programmer and the central proccessing unit of the computer. It is not possible under normal programming for the programner to tell the central processing unit - usually referred to as the CPU - what to do.

In the Sinclair machines the CPU is a Z80A chip, and I am sure it comes as no surprise to learn that the 280A does not understand a word of "BASIC"!

Indeed no CPU is able to be programmed in a way that is directly readable by humans.

If you think about it for long enough, you will realise that it would be impossible in any case to give a chip in a computer an instruction that would make any sense to a human. Take the top off your Sinclair and have a look at the chip marked "NEC" - this is the Z8OA CPU. Obviously this chip in your computer can only respond to electrical signals that are passed on to it by the rest of the circuitry!

The way this chip is designed, it can accept signals simultaneously fram eight of the pins connected to it.
Keeping in mind that what is really happening is electrical signals, we can still adopt a convention to represent these signals - for example showing a ${ }^{-1}$ if there is a signal, or a $0^{-}$if there is no signal.

A typical instruction might therefore look something like:
00111100
Quite a long way from something like
Let $A=A+1^{-}$,
for example, isn ${ }^{-1}$ it !
Nonetheless, this is what machine language is all about. The name says it all! It is a language for machines.

At this stage you may be asking yourself - if this is wat machine language programming is all about, why bother? Why not accept the benefits of someone else's work which allows us to program the computer in a language we can all understand, such as Basic or Cobol?

The Main Benefits Of Machine Language Are:
FASTER EXECUTION OF THE PRUGRAM
MORE EFFICIENT USE OF MEMORY
SHORTER PROGRAMS (IN MEMURY)
FREEUOM FROM OPERATING SYSTEM

All of the above benefits are a direct result of programming in a language that the CPU can understand without having to have it translated first.

When you program in Basic, the operating system is the program that is really being run by the machine. The program is something like:

NEXT Look at next instruction
Translate it into machine language Perform that instruction Store the result if required Go to NEXT again

This method of programming is up to 60 times slower than a program written directly in machine language!

Nonetheless, we would have to be among the first to admit that programming in machine language does have some drawbacks.

THE MAIN DISADVANTAGES OF MACHINE LANGUAGE ARE:

## PROGRAMS DIFFICULT TO READ AND DEBUG

IMPOSSIBLE TO ADAPT TO OTHER COMPUTERS
LONGER PROGRAMS (IN INSTRUCTIUNS)

## ARITHMETIC CALCULATIUNS UIFFICULT

This means that we must make a very conscious decision of which programming method we should use for particular applications. A very long program for financial applications should be written in a language designed to deal with numbers and one in which programs can be easily modified if required.

On the other hand there is nothing quite so bad as an arcade game written in basic - when you get down to it, it is just too slow.

Your own needs, the amount of memory in your computer, the time to put into programming, and so on will determine your choice of programming language.

## MACHINE VS. ASSEMBLY LANGUAGE:

There is only one major difference between assembly language and machine language: assembly language is more easily read by humans than machine language (but on the other hand, computers can ${ }^{-1}$ read assembly language).

Assembly language is a partial translation of machine language so that it can be read by humans in a form that is easier to understand than 01110111.

It is not an adaptation of machine language, such as BASIC. In assembly language there is one and only one instruction for each machine language instruction (and there is only one machine language instruction for each asssembly language instruction).

We therefore say that assembly language is equivalent to machine language.
Assembly language makes use of Mnemomics (or abbreviations). For example at this stage, the instruction

## INC HL

may not mean much to you, but at least you can read it. It you were told that "INC" is a standard abbreviation (or mnemonic) for increase and that HL is a variable, then by simply looking at that instruction you can get a feel for what is happening.

The same instruction in machine language is 23

Now obviously you can also "read" that instruction, in the sense that you can read the number, but it isn't going to mean much to you unless you have a table to look up.

Assembly language can be converted directly to machine code by a program or by you. The program is called an assembler, and we understand that an assembler for the $2 X 81$ is soon to be available.

Nonetheless, such assemblers typically require $6 K$ of memory, and this is not going to be much use if you have only l-4K of memory.

You will have to do the translation of mnemonics by hand, using the tables provided in this book.

It"s hard, it"s frustrating, it"s inconvenient, but it"s wonderful practice and gives you a great insight into the way computers work.


## WHAT IS THE CPU

If we want to talk the same language as the CPU we have to know what sort of a person the CPU is. Eventually you may be asking the CPU to do some quite remarkable tasks fram playing chess to keeping your books of accounts.

The CPU is no big mystery. I like to think of the CPU as a lonely little fellow, sitting in the middle of your Sinclair, being asked to do things all the time.

Especially calculations.
But the poor fellow doesn't even have a piece of paper and pencil to keep track of what is happening. How does he do it?

Let us look at one example in more detail - say you want the CPU to work out the time in New York, knowing the time in London.

Now given that the CPU doesn't know anything, first of all you tell it what the time in London is: $100^{\prime}$ clock. The CPU has nowhere to keep this information and doesn't know what you will ask it to do next, so it puts that information away in a box, say box \#1.

Then you tell it the time difference, say five hours earlier, and it puts that away in box \#2.

Comes the time for calculations, it races across to box \#1, gets the number, goes to box \#2, performs the calculation, and puts the result away, say in box \#3.

$$
10-5=5
$$

The answer of course is 50 clock.

All of this racing between boxes, adding, subtracting and so on would be extremely tedious if the CPU had to do it all in its head, so it does exactly what you or 1 would do - it counts on its fingers and toes.

The CPU's hands and feet are called Registers
The $\mathbf{Z 8 0}$ chip is remarkable among CPU's in that it has a lot of hands and toes - but we will get to that later.

In our time difference analysis above, we actually skipped a step when we just glibly said "performs the calculation".

The example is one you might be able to do in your head, but if you were given two large numbers to add without the benefit of calculator or pencil and paper you might have some difficulty. So let's go back to our time difference example:

For simplicity's sake, let's call one of the CPU's hands "Hand A". How does the CPU manipulate the contents of the box 1 and box \#2? The following sequence is pretty close to what the CPU would actually do

* Count out the value of box \#1 on the fingers of Hand $A$;
* Subtract the contents of box \#2 from what he has already on his fingers;
* Look at the value on the fingers of Hand $A$ and store it in box \#3.

Now if this is what truly happens, there are some pretty phenomenal conclusions to be drawn from this:

1. The CPU would not be able to deal with a number like 11.53 - it could only deal in whole numbers.
2. The CPU would be limited in its calculations to whatever number it could count to on its fingers.

This is true!

The main consolation however is that the CPU has a lot of hands and feet and can keep count on each of them separately, and that it can count to 255 using only the 8 fingers of Hand $A$.

We will deal in the next chapter with the details of how the CPU can count up to more than 8 on each hand while we can only manage 10 using two hands! Suffice it to say that each hand can count to 255 and each foot can be used to count to over 64,000!

The time difference execise above has still not been represented in anything like the language the CPU understands - all we have done is describe the processes. Let us now use mnemonics (Abbreviations) to instruct the CPU at each step:

SETTING UP:
LD (BOX 1 ), 10
LD (BOX \#2), 5
CALCULATING:
LD A, (BOX \#1)
SUB $A$, ( $B O X$ 2)
LD (BOX 3), A
These instructions may seem a little terse at first, but after all menmonics are mnemonics. "LD is an abbreviation for "load" so that LD A, 1
for example, would mean load $A$ with 1 : that is count off 'one' on the fingers of hand $A$.

We also use a rather clever image in these menmonics by the use of brackets: the brackets are used to indicate we wish to deal with the contents of whatever is inside the brackets.

It should be fairly easy to remember this on a visual basis because brackets do look like they are meant to indicate a container.

So running through the mnemonics above, we load the contents of Box 1 and $\$ 2$ with 10 and 5 , ...etc... to get the final result of 5 in box 3 .

All of this is fairly simple to follow and I am sure you can understand
that while you are doing this calculation the numbers on hand "A" represent the time in New York. A minute later they may be used to represent the number of employees in a company, and at some other time how much money you have.

You may be used to the concept of variables from your BASIC programming, but this is a concept you must leave behind in machine language programming.

The fingers of Hand "A" are not a variable in the same sense as in a BASIC program. They are merely what the CPU uses to count with.

One of the big differences in programming in machine language and
programming in Basic is in fact this lack of variables.
It is always possible to store things away in the memory locations, or boxes as we called them in the above example. But these are not really variables either. They are however immensely useful, but no more than memory locations set aside for specific purposes.

Let us go back to the CPU and consider what happens if someone comes in to the room in the middle of a calculation? Embarrassing situation with fingers flying, all full of information that he can ${ }^{-t}$ afford to lose.

The polite thing to do would be to get up and shake hands, but what would happen to all those numbers? One solution would be to quickly write down all the numbers and store them in boxes. But then you would have to remember in which boxes you had stored the information - and where are you going to store the number that tells you where the information is?

Our CPU gets away with it by using one of those tall spiky things that some people keep bills, spare notes, etc. I am sure you know those stacks where you spike one piece of paper on and then the next, and so one. It's great if you want the top piece of paper only, but very inconvenient if
you want to see what's in the middle because you have to go through all the pieces stuck on the spike.

This little stack, however, is ideally suited to our CPU because it only wants to look at the top piece of paper. When the "interrupt" comes, he puts all the information on the stack, and as soon as the interrupt is over, the CPU pops the top piece of paper off and continues with its calculation.

In computer terminology we call this spike a "STACK". When we put a piece of information of the stack we "PUSH" it on, and when we retrieve the information, we "POP" it off.

All kinds of information can be "PUSH"ed and "POP"ed on and of $f$ the stack - for example if the CPU was in the middle of a complex calculation when the interrupt came, not only would it need to save whatever information it had on its fingers and toes but also what point of the calculation he had reached. This would involve many separate "PUSH"es and then many separate "POP"s at the end.

The stack is also extremely useful if the CPU runs out of hands.
For reasons best known to itself our CPU likes to keep the stack stuck to the ceiling just above where he is working. This means that the more information is "PUSH"ed on, the further the stack grows downwards.

The main advantage of the stack is that the CPU does not need to remember which box the information is in - it knows it is the last piece "PUSH"ed on the stack, because it has organised itself so that it would always be so.


We mentioned in the previous chaper that the CPU was able to count to 255 using only eight fingers. How can this be when with 10 fingers we can only manage to count to 10 ?

It is certainly not because computers are smarter (they aren $t$ ) but because the CPU is more organised in its information than we are: why should raising your index finger have the same value ( $={ }^{-} 1^{-}$) as having your little finger raised?

It seems obvious that if you so wished you could represent two different numbers in this way.

It is very much the same sort of thing as realising that the number 001 is different from the number 100. The plain truth is that humans are not very efficient in the use of fingers for counting.

The CPU understands that not having a finger is of some information and that which finger is raised is a valuable piece of information.

With only two fingers it ids possible to devise a way to count from 0 to 3, as follows:


```
We can indicate not having
a finger raised as \({ }^{-} 0^{-}\),
and having a finger raised
as \({ }^{-1}{ }^{-1}\) 。
this does not mean \(11=3\).
It means we chose to let
the representation 11 (or
two fingers) have the
value 3.
```

We could just as easily have chosen a different representation.
There is a direct relationship between this and binary representation. The $\mathrm{CPU}^{-}$s fingers are locations in memory and they can be made to indicate on and off (or ${ }^{\prime} 0^{-}$and ${ }^{-1} 1^{\text {' }}$ as convention dictates).

If we added a third finger to our example above we could represent all the numbers from 0 to 7. Three fingers for $0-7$ !
Four fingers would be able to represent all the numbers from 0 to 15 !
In order to simplify the notation of such numbers, and to avoid confusion in trying to write down the number eleven as opposed to indicating that two bits were set, a universal convention has been adopted:

The numbers 10 - 15 are indicated by the letters $A-F$.

Decimal $10 \Rightarrow A \quad$ (We show $\Rightarrow$ as ${ }^{*}$ equal")
$11 \Rightarrow B$
$12 \Rightarrow C$
$13 \Rightarrow D$
$14 \Rightarrow E$
$15 \Rightarrow F$
Simple isn ${ }^{-1}$ it?
This way of treating numbers is called the Hexadecimal Format.
In machine language programming, it is convenient to deal with mumbers in a Hexadecimal Format.

This is only a convention and if you so wished you could write all your instruction in normal decimal format. Naturally you would need a program to convert the decimal notation to binary bits being on and of $f$. But this is not a major problem because we use a program to convert the hexadecimal notation to binary bits.

It is convenient for us to use the hexadecimal format because:

1. It is easy to convert from this form to binary, which tells us which bit (or finger) is doing what.
2. It gives us an easy means of seeing whether numbers are 8 -bit or 16-bit.
3. It standardises all numbers to sets of 2-digit numbers.
4. It is the common convention and familiarity with hexadecimal will allow you to read other books and manuals more easily.

But it is only a convention and not a sacred rule.
The hexadecimal system as we mentioned earlier, lets us represent the numbers 0 to 15 using only 4 bits. Any 8-bit nemory location or 8-bit register can therefore be described by two sets of 4 bits.
(This is the same as saying that any combination of 10 fingers can be represented by two hands of 5 fingers each).

The reason we are concerned with 8 -bit memory locations and 8-bit registers is that this is the structure of the Sinclair Computers. All memory locations and all single registers have 8 bits.
(This is not hard to conceptualise - it's like saying all humans have 5 fingers on each hand).

Taking things one step at a time, let us became familiar with 4 fingers first:

$$
\begin{aligned}
& \{V \sqrt{n} \\
& 1111=8+4+2+1=\text { Decimal } 15 \\
& =F \quad \text { (In } \\
& \text { Hexadecimal Notation) }
\end{aligned}
$$

For those of you with a mathematical bent, you may notice that the number each finger represents is multiplied by 2 as you go to the left. If we number the fingers:

$$
\int_{3} \int_{2} \prod_{1} \int_{0}
$$

Then the value of each finger is ${ }^{-2}$ to the power $N^{-}$where $N$ is the finger number. Let's call a 4-finger hand a "Handlet" (just as a small cigar is a cigarette?

To prevent confusion, some people write " H " after a hexadecimal number (eg. 10H). The " H " has no hexadecimal convention.

## EXERCISE:

What decimal and hexadecimal value do the following arrangement of bits (or fingers) represent?

DECIMAL HEXADECIMAL
0010
0110
1001
1010
1100

It is important for you to become familiar with the hexadecimal convention, and if you had difficulty with the concept, do read the last few pages again before going on.

Let us examine what happens if we want a number greater than 15 ? Say 16? We would use the next finger on the left, as:

$=16$ Decimal $=10 \mathrm{H}$ (Hexadecimal)
The reason we write the number as $10 H$ is that we divide the hand in two "4-Bit Handlets". We can therefore easily denote each handlet by one of the hexadecimal numbers representing $U$ to 15 ( $0-9 \& A-F)$.

In this way any 8-Bit hand can be written as exactly two hexadecimal handlets:


The "Handlets" on the left indicates 16 times as much as the "Handlet" on the right. This is much the same waylaslin decimal notation. The digit in the "tens" column is worth ten times as much as the digit in the "ones" column.

We convert numbers in decimal format such as 15 automatically to:
$15=(1 * 10)+5$
This is so automatic that we don ${ }^{-t}$ even think about it.
It is exactly the same thing in hexadecimal notation. To convert back from hexadecimal notation to decimal notation, we multiply the hexadecimal number on the left "handlet" by 16. Using the example above:

$$
\begin{aligned}
10 \mathrm{H} & =(1 \star 16)+0 \\
& =16 \text { Decimal }
\end{aligned}
$$

This is how we are able to count to 255 using only 8 fingers. The maximum is obtained when all fingers are held up:


The smallest number is when no fingers are held up:

$$
00 \mathrm{H}=0 \text { Decimal }
$$

Note that all numbers, from the smallest to the largest require 2 and only 2 digits to define the number.

Try out for yourself any conbination of 8 digits and see if you can convert it to hexadecimal notation, and then into decimal notation.

It may seem a little strange and awkward at first, but you will soon get the hang of it.

Also that when you count in hexadecimal, you do the same as in decimal:
Decimal: $26 \quad 27 \quad 28 \quad 29 \quad 30$ Etc.
Hexadecimal: $\begin{array}{lllllll}26 & 27 & 28 & 29 & 2 A & 2 B & 2 C\end{array}$
$2 D \quad 2 E \quad 2 F \quad 30 \quad E t c$.
The values of the numbers in the decimal and hexadecimal series above have different values of course. Note that after 29 H you get 2 AH , no 30 H !

## NEGATIVE NUMBERS

The last chapter showed you how it is possible to represent the numbers 0 to 255 on the fingers of one hand.

I also said that the $\mathbf{Z 8 0}$ chip was mainly designed for operations on one hand (that is 8-bit operations) - in other words, although some instructions allow you the use of two hands thus giving a number range of 0 - 65,535 ) most of the work will be done in registers and memory locations that only allow a number range of 00 - FF (in hexadecimal notation).

What about negative numbers?
Life would indeed be limited if we couldn ${ }^{-1}$ represent negative numbers!
Obviously we have to have some representation of negative numbers, so let's say that a number on our hand is negative if we hold our thumb up. (In computer terminology that is saying that the highest bit - bit 7 - is on).

That means the highest number we can have is not as high as before, because we can no longer say that holding all fingers up will show 2b5: for a start we have agreed that this will be a negative number. In fact, half the numbers will be negative and half will be positive(depending on whether the thumb is up or not).

The total number range possible on one hand if we allow negative numbers will be from - 128 to +127 . (Note that the total number range possible to be represented will still be 256 numbers).

Now comes the crunch: when is a number with the thumb up a large positive number and when is it a negative number?

The answer, as strange as it may seem, is whenever you feel like it!

We have to make a choice: numbers can either be in the range of 0 to 255 or in the range - 128 to +127 . They can ${ }^{-1}$ be both at the same time! It is up to you, the programmer, to decide which convention you are using at a particular time.

All the instructions will work equally well, whether you choose to let the numbers contained in the registers or memory be all positive or positive and negative.

## CHOOSING A REPRESENTATION:

We need a representation of negative numbers, such that, all instructions will work and that when a number is added to its negative we get zero.

Let's think about the number which when added to 1 gives us zero: (we already know that the thumb - bit 7 - will be up)

$$
\begin{array}{cccccccc}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
1 & ? & ? & ? & ? & ? & ? & ? \\
\hdashline 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{array}
$$

Lets try the number $10000000001-i . e$. the same as the positive number but with the thumb up:

$$
\begin{array}{llllllll}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
\hdashline 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0
\end{array}
$$

This is obviously not the right answer! We need a number that will take that carry from bit 0 , and convert it to zeros all along.

You can try to do it yourself, and you will see that the only nunber which will give us the right answer is $1 \begin{array}{llllllllllll} & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & \text { (FFH } & \text { in }\end{array}$ hexadecimal).


Trying to think of a rule which will produce the negative, it looks as if though we have to get the opposite of the number and add one at the end.

Let's try this rule on another number, such as 3 , say:
3 =
Opposite
Add 1 =>
00000011
11111100
11111101
(FDH)
Let's add this number to 3 and see what happens:


It works!!
We have found a way to represent negative numbers!

$$
\begin{array}{ll}
-01 \Rightarrow & \text { FF } \\
-02 \Rightarrow & \text { FE } \\
-03 \Rightarrow & F D \text { and so on. }
\end{array}
$$

The largest positive number is
$01111111=7 F \Rightarrow 127$ Decimal
And the negative of this is
$10000001=81 \Rightarrow-127$ Decimal
The real test of this rule is to see if by applying the rule to a negative number we get back the positive again! Let's try it out on -3 which we worked out above is FOH.

Number $\quad 11111101$
Opposite 00000010
Add $1 \Rightarrow 000000011$
This is therefore a representation that works! We can apply it any number, whether positive or negative, and get the negative of that number.

Exactly the same reasoning applies to 16 -bit numbers, except that it is the thumb of the high byte which is set to on to indicate the negativeness of the number. (ie. bit 7 of the high byte).

Convention:

Remember that this is only a convention! You still have to decide at all times whether the numbers you are using are meant to designate numbers in the range 0 to 255 or numbers in the range - 128 to +127.

Exercise
 represented in this convention, how would you represent - 128?

## PROPER NAMES FOR THE CPU'S HANDS AND FEET

The images we have been building up of hands, feet and boxes make the processes easy to visualise and are a good representation of what is going on, but computer buffs tend to look askance if you say things like
"... and then the computer shifted its information from its right hand to its left hand."

We will now give you the proper names for the CPU's hands and feet. So that when faced with that situation, you will be able to say:
"LD B,A!"
To start off with, computer buffs refer to the hands and feet of the CPU as "REGISTERS".

We mentioned earlier that the CPU has eight hands: these are called $A, B$, $C, D, E, F, \ldots$. In our world, the definition of a hand is something with eight fingers.

The CPU also has two feet: these are named $I X$ and $I Y$. The definition of a foot is anything with 16 toes!

The naming of hands and feet is fairly easy to follow becase if a register has only one letter in its name then it must be a hand (that is, contains 8 bits), while if it has two letters in its name then it must be a foot (that is, have 16 bits).

Did you notice the smooth transition from fingers and toes to bits? We will have you used to computer terminology in no time.

Actually the remaining two hands for the CPU after D,E,F,...are not named " $G$ " and " $\mathrm{H}^{\prime}$ as one would expect but " H " and "L".

The conventional way to represent all these registers is as follows:


Notice that "F" is paired with"A", but after that the rest follow fairly naturally. The reason that registers are paired in this way is that it is sometimes possible to make a foot out of two hands!

After all, if the definition of $a$ foot is something with 16 bits, then maybe we can fake it from time to time and use two 8-bit hands to do the work of a foot. We therefore talk about "Register Pairs" such as BC, $D E_{2}$ and $H L$.

The reason the register pair "HL" was called "HL" instead of something like "GH" was to help people remember which of the two registers had the high number and which had the low number.

It's as if though you wished to represent the numbers 0 to 100 on your hands and toes. You can easily set up you fingers to represent the numbers 0 through to 10 , and similarly with your toes (assuming that you are agile enough). One way you could denote the numer 37 in this way would be to count off 3 on your fingers and 7 on your toes. But there has to be some agreement on which is the high number and which is the low number otherwise someone else might think you meant to represent the number 73.

The "H" in "HL" stands for high and the "L" stands for low, so there is no chance of confusion - right?

This diagram of register pairs also serves to indicate which register in the other register pairs contains the hight number:
$B$ in BC
D in DE
Because all the high and lows are treated in the same order.
The feet (IX and IY) also have a special name: they are called "Index Registers". This has a lot to do with the fact that they can be used to organise information in much the same way as a book index is organised.

OK, now that you understand the terminology, here are some special points:

## FLAGS:

Please note that "AF" is not usually treated as a register pair. The "F" in this case is used to denote "Flag Register", and we will be dealing with this in a separate chapter.

## ALTERNATE REGISTER SET:

I thought that this might be a nice place to mention that the CPU also has a spare set of hands!

Not really so much a spare set of hands (all right, alternate register set, if you want the proper terminology), as a spare set of work gloves.

It's as if though you had a set of stiff plastic gloves, so stiff in fact that they retained the shape of your hand when you took them off. If you had counted of $f$ the number 3 on your hand for example and took of $f$ your gloves, then the glove would still retain the shape of a hand with the number 3 counted of $f$ !

You can no doubt think of uses for such gloves immediately - you could make a note of a number While wearing one set of gloves, swap gloves

and the old number would still be there when you needed on the other set of gloves!

The other glove is there if you want to use it and it won't forget the impression of your hand when you took it off. Unfortunately you can't just glance down and see what was the number you had retained there. Nor, naturally, can the glove perform any calculations without a hand inside the glove!

You actually have to swap gloves again to be able to use whatever information the gloves retain.

The CPU has a spare set of gloves for each pair of hands (but not for feet - who ever heard of gloves for feet?) But they are not interchangeable between hands, just as you can't put a left glove on a right hand.

The representation of all the registers is now therefore:

| $\mathbf{A}-\mathbf{F}$ | $\Leftrightarrow==>$ | $A^{\prime}-\mathbf{F}^{\prime}$ |
| :--- | :--- | :--- |
| $\mathbf{B}-\mathbf{C}$ | $\Leftrightarrow==>$ | $\mathbf{B}^{\prime}-\mathbf{C}^{\prime}$ |
| $\mathbf{D}-\mathbf{E}$ | $\Leftrightarrow==>$ | $\mathbf{D}^{\prime}-\mathbf{E}^{\prime}$ |
| $\mathbf{H}-\mathbf{L}$ | $\Leftrightarrow=>$ | $\mathbf{H}^{\prime}-\mathbf{L}^{\prime}$ |

IX
IY
Whichever set of gloves you are wearing has the same name as the hand it is for, while the spare set is always indicated with the dash symbol.

The instructions still relate to what the hands are doing, not to which pair of gloves you have on. So although we show the spare set with a dash, there are no instructions such as LD A', 1.

The only instructions involving the alternate register set are of the "swap gloves now" type. For example:

1. LD A, (Box \#1) ; load A with contents of box 11
2. EX $A F, A F{ }^{\prime}$
short for exchange fe. swap gloves on AF
3. LD A, (Box \#2)
4. EX AF,AF' ; another exchange
5. LD A, (Box \#3)
;

You will note that in the previous 5 instructions there are no instructions which have specifically affected the alternate register set but we have without doubt altered their contents.

This example is designed to illustrate the concept of the alternate register set. Try to work out what is happening. No you know what will be in register " $A$ " after each instruction?

For simplicity's sake, Let's assume that the contents of the three boxes are as follows:

| $($ Box $\# 1)$ | $=1$ |
| :--- | :--- | :--- |
| Box \#2) | $=1$ |
| Box $\# 3)$ | $=3$ |

Then the following is what happens after each instruction:
REGISTER A REGISTER A'

| 1. | 1 | Not known |
| :--- | :---: | :---: |
| 2. | Not known | 1 |
| 3. | 2 | 1 |
| 4. | 1 | 2 |
| 5. | 3 | 2 |

Really quite simple isn't it?

THIS IS ALL VERY WELL, BUT
HOH DO I RUN A MACHINE LANGUAGE PROGRAM?
You have probably heard enough about the CPU and hexadecimal notation, but all this seems so irrelevant. It doesn't explain how you actually ( $R * U * N$ ) a machine language program.

The Sinclair $\mathbf{Z X 8 0}$ and Sinclair $\mathbf{Z X 8 1}$ are actually running machine language programs all the time! (when they are on). It's just that you are not aware of it. Even when you're not doing anything, just watching the screen, trying to think of what to enter as the first line of your revolutionary Basic program, the Sinclair computer is busy running under the control of a machine language program.

This program is one that is stored in the "ROM" chip and is referred to as 'The Operating System'. For example the part of the program that is running when you're sitting there looking at the screen does the following things:

> Scan the keyboard for entry Note that no key has been pressed Display the present screen (empty)

Incidentally this is why the screen will flicker when you finally do press a key because the CPU goes on to trying to figure out what to do now that you pressed something. It can't do two things at once, and the one that suffers is the display of the screen.
(Except in the $\mathrm{ZX81}$ SLOW mode - This is because there is another little fellow in the hardware who taps the CPU on the shoulder every so often and reminds the CPU that it's time to display the screen again. Really).

Even when you are running a 'Basic' program, the CPU is still under the instruction of the machine language program. This program is of the 'INTERPRETOR' type: It looks at your next Basic instruction, converts it to machine language, executes that part of the program, and then returns to interpret the next instruction.

All this stops being true when you run your own machine language program!
Total freedom from the operator system! The use of the 'USR' function hands over total control of the CPU to whatever commands you have placed at the USR address.

This can be pretty terrifying as you could lose everything stored in memory if you lose control. One error and you will have to turn the Sinclair off and start again from the beginning.

There are no error messages to catch what you have done, no syntax checking for incorrect statements - so if you make the slightest error, the hours of work you put in to enter your program could be lost!

At the end of this book we have included a 'BASIC' program which will allow you to enter and edit machine language programs. Once you have entered this program on your Sinclair, store it on tape as it is more than likely that you will lose control of your machine language program at least once.

On the other hand do not be afraid to experiment - you cannot damage the computer with any machine language program you enter. The worse that happens is that you may have to turn the Sinclair off and on again.

We will now just whet your appetite with the very simplest possible machine language program. Load the 'BASIC' "Machine Language Editor" found at the back of this book and press "RUN".

The program will ask you for a starting address where you wish to enter your program. Choose an address beyond the end of the space used by the editing program and the variables, such as 17300 for the $2 X 80$, and then press "NEW LINE".
(Users with Additional Memory could choose any address beyond the space occupied by the program, the display space and the variable storage, such as 19000 , say.)

Note 2 X 81 : 1 K users - due to the extreme space limitations in the $2 \times 81$ version, there is effectively no free memory after the machine code editor program has been entered.

Nonetheless it is possible to enter and run machine language programs by using the printer buffer area which starts at 16444.

Note that in the $2 \times 81$, whether additional memory is available or not, all code poked into free memory will be cleared between "RUN's. (Even using -GOTO does not solve the problem).

The same is true for code poked into the printer buffer area.
Once you have entered the machine code editor program and pressed (RUN), the screen will now show:

| MEMORY | CODE |
| :--- | :--- | :--- |
| 16444 | $00 \quad(2 X 80$ users. use 17300) |

Now enter "C" and "9" then press "NEW LINE". the screen should now show:
MEMORY COUE
$16444 \quad 00 \quad$ C9 ( $2 \times 80 \quad \Rightarrow 17300$ )
CHANGES?

What the screen display is showing you is the old value at location 16444 ( = 00 ), then the new value at location 16444 ( = Cy which you have just entered) and then asks you whether you want to make any changes to what you have just entered.

At this stage you do not want to make any changes, so just press "NEW LINE". (To make changes enter " Y " or "YES" or "YEACH" or any other word that starts with "Y").

Congratulations: you have just entered a one instruction machine machine language program.

What the instruction "C9" means is : RETURN.
It's a little like riding a bicycle for the first time: you really want to be let loose on your own, but as soon as you go a little way you want to "RETURN" to the safety of earth (or operating system as the case may be).

So after you pressed "NEW LINE" above, the program will ask you:
CHANGES?
MORE?
The program wants to know if you have any other code you want to enter. Again it's looking for a positive answer and pressing "NEW LINE" will allow you to exit from the program.

The editing program has now finished.
Now we run the machine Language Program:
The program will ask you for the starting address of your machine language program. Enter the starting address where you "POKE"d the machine code:

16444
(OR 17300 FUR ZX 80 USERS)
(Users who chose a different address should make the appropriate change).

Press "New Line" for the running of your first machine language program.
What happened? Why did the screen come up with 16444 or 17300 or whatever address you used as the start?

The answer lies in the way the Sinclair operating system (yes the same one) deals with the "USR" function.

When the operating system encounters the "USR" function it loads the address the user specified into the register pair $H L$ for the $2 \times 80$ - in this case 173000.
The value of "USR", as in
Let $A=U S R$ (17300)
is the value of the register pair $H L$ on return from the subroutine.
Since our short machine language program did nothing but go and return,
the value of HL was unchanged, and the statement
Print USR (S17300)
Naturally gave the answer 17300!
This feature of the "USR" function will prove to be a very useful one as it will enable us to monitor what is happening during the running of a machine language program.

In the case of the $Z X 81$, it is the value of the " $B C$ " register pair which is returned by the "USR' function, but the concept is exactly the same.

Let us enter the following machine language program: (press "Run" if you still have the listing of the "Maching Language Editing Program" on the screen)

MEMORY CODE
ZX 80 USERS ONLY:

| 17300 | C9 | 2B |
| :--- | :--- | :--- |
| 17301 | 00 | C9 |
|  |  |  |
| Changes? | More? |  |

The way to enter this short two-instruction program is as follows:
Enter " 17300 " in response to starting address query Enter "2B" followed by "New Line" when the screen shows "17300 C9"
Enter "C9" followed by "New Line" when the screen shows "17301 00"
Enter "New Line" in response to "Changes?" and to "More?"
The enter " 17300 " in response to "Start For USR?" and press "New Line".
This time the result will be 17299! This is because the instruction " $2 B$ " is "DEC HL." (abbreviation for decrease value of HL by 1).

2X 81 USERS ONLY:
Enter your program in exactly the same way as above, but change the code to be entered to the following:

| 16444 | 00 | OB |
| :--- | :--- | :--- |
| 16445 | 00 | C9 |

Start for USR? 16444
The concept is again the same, but this time we use an instruction which relates to the " $B C$ " register pair rather than to the "HL" register pair ${ }^{-} O B^{-}$means ${ }^{-} D E C B C^{-}$.

You will have noticed a few things about this machine language editing program:

The first column under the heading "Code" shows what is in that location before you make your changes.

The second column under "Code" shows what is in that location after you have tried to make your changes.

The question "Changes?" only came up after you entered "Cy" into a location

The following features are some that you would not yet have discovered:
Pressing "New Line" after being shown the contents of a location leaves that location unchanged.

The question "Changes?" will also come up after 20 locations have been displayed. ( $2 X 81$ users program has been designed to show only 10 locations due to the memory limitations of the $1 \mathrm{~K} \mathbf{Z X} 81$ ).

Should you answer "Yes" to the question "Any Changes?" then the screen will clear and the program will start again at the first location. The first column under "Code" will now show the contents of the locations as they now exist (i.e. after your changes).

If you have no changes to make, just keep entering "New Line" until you get to the location you want to change, and change the contents in the same way that you have already done.

If you answer "Yes" to the question "More?" the screen will clear and a new set of locations will be displayed.
**NOTE:**
The last location of the previous page will now be displayed at the top of the page. Don ${ }^{-t}$ make the mistake of entering something new at location if you have already got what you want there!

Experiment with looking at different locations and trying to change the contents of different menory locations. Remember you can ${ }^{-t}$ hurt the system - the worse that can happen is your screen will go black and will have to turn off the Sinclair and turn it on again.

If you do not want to ( $R^{*} U * N$ ) a USR program after changing or looking at the contents of memory, enter "XX" as reply to "Start for USR?"

## EXERCISE:

Try entering "0" as your starting address (beginning of RUM). What happens when you try to change the contents of the memory locations? Why?

## EXERCISE:

Try examining the first line of the screen display. What happens when you change the contents of one of the locations? What happens when you enter "76"? Why?

## LOAUING UPERATIONS

| Mnemonic Bytes |  | Time Taken | C | $Z^{\text {Effect }}$ | $\begin{gathered} \text { on } \\ \text { S } \end{gathered}$ | $\underset{N}{\text { Flags }}$ | H |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LD Register, Register | 1 | 4 | - | - - | - | - | - |
| LD Register, Number | 2 | 7 | - | - - | - | - | - |
| LD A, (Address) | 3 | 13 | - | - - | - | - | - |
| LD (Address), A | 3 | 13 | - | - - | - | - | - |
| LD Register, (HL) | 1 | 7 | - | - - | - | - | - |
| LD A, (BC) | 1 | 7 | - | - - | - | - | - |
| LD A, (DE) | 1 | 7 | - | - - | - | - | - |
| LD (HL), Register | 1 | 7 | - | - - | - | - | - |
| LD (BC), A | 1 | 7 | - | - - | - | - | - |
| LD (DE), A | 1 | 7 | - | - - | - | - | - |
| LD Register, ( $1 X+D)$ | 3 | 19 | - | - - | - | - | - |
| LD Register, ( $\mathrm{I} Y+\mathrm{D}$ ) | 3 | 19 | - | - - | - | - | - |
| LD (IX+D), Register | 3 | 19 | - | - - | - | - | - |
| LD (IY+D), Register | 3 | 19 | - | - - | - | - | - |
| LD (HL), Number | 2 | 10 | - | - - | - | - | - |
| LD ( IX +D$)$, Number | 4 | 19 | - | - - | - | - | - |
| LD (IY+D), Number | 4 | 19 | - | - - | - | - | - |

## COUNTING OFF NUMBERS

ON ONE HAND
Since everything in the Sinclair CPU is designed around 8-bit hands or 8 bit memory locations, it is obviously of major importance to learn how to count of $f$ numbers on one's hands.

Just which operations are allowed and how easy they are to do is the key to machine language programming.

Imagine for a moment that you are the CPU: obviously like most people, you are right handed and there are things you can do with your right hand that you are not quite so adept at with other hands. The equivalent hand on the CPU is the " $A$ " register.

This is the only one where you can do the complicated tasks of adding and subtracting.

On the other hand (so to speak if you"ll forgive the pun) you can temporarily store what you have in your right hand onto any other hand and vice versa.

Computer boffins refer to this as Register Addressing.
But that is just a big name for saying transfer information fram one register to another. Examples are:

$$
\text { LU } A, B
$$

LD H,E and so on.

Please note the terminology inolved: "LD" means "Load", "," means "With", and the mnemonic (abbreviation) instruction is read in the same order as an English sentence.

We would thus read out loud something like:
LD $A, B$
as "Load $A$ with $B$ ". The next example would be read as "Load $H$ with $E$ ".
We can swap from one hand to any other hand as we mentioned earlier. The exception that proves the rule is the "F" register which we should not think of as a hand at all. It is as we mentioned earlier the "Flags" register and does not store numbers in the normal sense.

Apart from that exception you can manpulate any hand to any other hand. Even the seemingly stupid instruction "LD $A, A$ " is permitted!

A short shorthand of this is "LD $r, r$ " where " $r$ " represents any 8-bit register except "F".
0.K: we now know we can shuffle information between hands, but that's not going to do us much good without some original information on those hands.

The second way that we can count off numbers on our hands is for us to specify how many we want the CPU to count of $f$ on which hand!

For example, count off 215 on hand " $D$ ". I am sure you know enough about the mnemonics by now to be able to write this as:

LD D,D7
(D7 is the hexadecimal representation of 215).
This is called IMMEDIATE ADDRESSDSIMG.
(Pretty obvious isn ${ }^{-t}$ it?).
Once again you can do this with any of the registers, with ary numbers whatsoever.
(The limitation being of course the size of the nymber you can specify with 8 bits: 0 - 255).

A short shorthand of this is "LD $r, n$ " where " $r$ " indicates any register and " $n$ " any number. The previous convention of one letter $=$ " 8-bits still applies.

Now we're staring to get someplace: we as programmers can now specify which numbers get loaded onto which registers and we can spin them around. But we still haven't learnt how to put any of these numbers away in memory locations, and there are only so many registers!

As soon as we leave the internal registers the CPU is no longer 'At Home'. We therefore call putting something away in a memory location "External Addressing".

We showed you very briefly an example of this when we were doing the time difference exercise:

LD A, (Box *3)
The general mnemonic for this is:
LD A, (nn)
Don't forget that in our shorthand the brackets imply "The Contents Of".
Note two things about this:

1. You can only do it with Register $A$
2. You have to supply the number of the box as a $\mathbf{1 6}$-bit number.

The reverse instruction is also valid. This is one thing you will notice about the 280 - there is a certain symmetry about the instruction set:

LD (nn),A
Do notice that these instructions only apply to Register "A" - there will be times when you will wish for such instructions involving the other registers.

Let us pause here for a second and consider what these two instructions actually mean and do for us.

In the first place, the maximum number that can be defined by the number nn is a little over $\mathbf{6 4 , 0 0 0}$. This means that the maximum memory possibly reached by this instruction is only 64K! In fact on the Sinclair machines, because of the hardware construction everything over 32K is not available to the user.

This means that all the memory - ROM, Program, Display, and free memory have to fit in 32K:

The first 8 K are reserved for the ROM.
The second 8 K are a copy of the 1 st 8 K as a result of the hardware design
The last 16 K are the maximum RAM possible.
The instruction "LD A, $(\mathrm{nn})$ " - which is read as "Load A with the contents of location nn" - is a very powerful instruction. It enables us to "Read" the contents of any memory location, whether in ROM, or RAM.

You can use this instruction to explore to your heart's desire, even to a location where there is no memory - e.g. to try to see what is beyond the IK RAM memory even if you do not have additional memory. You will be surprised - it is not all zeros!

The reverse instruction "LD (nn),A" - which is read as "Load the contents of memory location nn with $\mathrm{A}^{\prime \prime}$ - will attempt to write to any memory location as well, but will be restricted by the physical limitations: You can ${ }^{-1}$ write to a location that can ${ }^{-1}$ store that information, such as memory beyond the size of your system or into ROM space.

Another consequence of this instruction is that we have to know at the time of writing the program which memory location we wish to examine or write into. The abbreviation "nn" means a definite number - e.g. 17100 and not a variable.

You can"t use this instruction in the machine language equivalent of a "FOR - NEXT" loop. The main use for this instruction is therefore for setting aside particular memory locations as variable storage. E.g. define $17000=$ Speed
$17001=$ Height
$17002=$ Fuel Left
In a lunar lander type program.
You could therefore plan a program where you got the fuel left, decreased it, and stored the new amount of fuel back into that location. You will know at the time of writing your program the address of that memory location which serves to act as a variable.

Let us be clear about this. Location 17002 is not a variable. It is only a memory location which you use to store certain information.

When writing your program you would therefore write something like LU A, (Fuel)
and when you or the assembler got to specifying the actual machine code for this instruction you would replace "Fuel" by the hexadecimal address of the memory location you specified.


But what if we don ${ }^{-t}$ know the exact address of the memory location where the information we seek is. Suppose we can only calculate where that information is going to be? Because we need 16-bits to specify the address of any memory location, we would need to store it in a 16-bit register: this means one of the register pairs $B C$, $D E$, or $H$, or one of the Index Registers IX or IY.

One way we can do this is to have one of the register pair contain the address of the memory location. Because the register contain the information and because we don ${ }^{-1}$ have the address directly we call this form of addressing Register Indirect Addressing.

The memonic abbreviations for these are
LD $\mathrm{r},(\mathrm{HL}$ )
LD A, (BC)
LD A, (DE)
The English reading of these instructions is
"Load the register with the contents of the memory location pointed to by $H^{\prime \prime}$
"Load $A$ with the contents of the memory location pointed to by $B C "$
"Load $A$ with the contents of the memory location pointed to by DE".

Note that by using "HL" as the pointer to our memory location we can load to any register - even $H$ or $L$, as strange as that may sound - but that using $B C$ or $D E$ we can only load into the $A$ register.

This is because the HL register pair is the favoured register pair in the same way that the $A$ register is the favoured single register.

Once again there is a symmetry to these instructions and we can store information into memory locations in a similar way:

$$
\begin{array}{ll}
L D & (H L), r \\
L D & (B C), A \\
L D & (U E), A
\end{array}
$$

This is still called "Register Indirect Addressing" whichever direction the information flows in.

Alternatively we could use the Index Registers IX and IV to point to the memory location. This is where we will find out why they are called Index Registers and I am sure it will come as no surprise to you that this kind of pointing is called INDEXEU ADURESSING.

The reason that they are called Index Registers is that we can use them as pointers to an entire table of items, such as the lst item, the 10th item, the 137th item and so on.

The short shorthand is:

$$
\begin{array}{ll}
L D & r,(I X+d) \\
L D & r,(I Y+d)
\end{array}
$$

" $r$ " is again any register, and " $d$ " is the "displacement" fran the address pointed to by IX or IY. (Don't get the use of "d" confused - we don ${ }^{-1}$ mean register " $D$ " but $d=$ displacement).

The number "d" is an 8-bit number which has to be specified at the time of programming and cannot be a variable. This is the weakness of this particular instruction and means that its use, is usually limited to reading and writing tables containing data.

The symmetrical instruction is also available:
LU (IX + d), r
LU (Ir + d),r
If this particular mode of addressing sounds a little complicated, don ${ }^{-} t$ worry: it is not a very commonly used instruction and you are unlikely to need it in your first few programs.

The $\mathbf{Z 8 0}$ chip used in the Sinclair Computers is nothing if not versatile, and you can combine some of the ways of loading numbers we described above.

For example, you can combine immediate addressing (i.e. specifying the number you want loaded) with external addressing (i.e. specifying the address to be loaded by using a register pair).

This is called - surprise, surprise - "IMMEDIATE EXTERNAL ADDRESSING".
Unfortunately you can only use the $H$. Register Pair and the short shorthand is therefore:
LD (HL),n

This is useful as you can directly fill a memory location without first having to load the value in a register.

A similar combination is possible with the Index Registers, called "IMMEDIATE INUEXEU ADURESSING".

This is of more limited use, and the abbreviated form for these instructions are:

$$
\begin{aligned}
& \text { LD } \quad(I X+d), n \\
& \text { LU } \quad(I Y+d), n
\end{aligned}
$$

## USING THESE INSTRUCTIONS IN

A MACHINE LANGUAGE PROGRAM
Let's try to put some of these "LU" instructions into practice.
We know from the previous chapters that after returning fran a "USR" machine language program the value of the "USR' is the contents of H. Let's run the following program:

MEMORY COUE
FOR ZX 80 USERS:

| 17300 | 00 | $2 E$ |
| :--- | :--- | :--- |
| 17301 | 00 | 00 |
| 17302 | 00 | C9 |
|  |  |  |
| Changes? | More? |  |

FOR $2 \times 81$ USERS:

| 16444 | $O O$ | OE |
| :--- | :--- | :--- |
| 16445 | 00 | 00 |
| 16446 | 00 | C9 |

From now on, we will no longer be showing you machine language programs in this way as it is a cumbersome method and does not allow you, the user, to understand the point of the program.

We assume that by now you have enough familiarity with the basic "Machine Language Editor" to be able to enter program. We will therefore be showing all of our programs as follows:


This notation gives you the machine codes on the left side and the

Z80 assembly memonics in the right hand column. It also indicates very clearly which instructions require only a single byte (such as return) and which instructions require 2 bytes, etc. (Some instructions on the $\dot{Z} 80$ can take up to 4 bytes!).

The other point is that we shall try to make all our program independent of origin so that it does not matter what you specify as your starting address.

Nonetheless remember that these programs are designed to be entered with the "Machine Language Editor" program at the back of the book or any other loading program you may design yourself.

Before running this program what do you expect the result to be?
The program sets the "L" register in the register pair HL to zero, and you know that HL starts of $f$ with the address of the program, say 17100.

Will the answer be $2 \times 80$ : $2 \times 81$ :
A. 0000 A. 0000
B. 17300
B. 16444
C. 16896
C. 16384

Now run the program. Was the answer what you expected it to be?
If you are unclear about why the answer was what it was go back and reread the chapter on "The Way Computers Count".

Now try running the following program:

| ZX 80 Version |  |  | 1 | 2X81 Version |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 26 | 00 | LD H,O | 1 | 06 | 00 | LU | B,O |
| 2 E | 00 | LD L, 0 | $!$ | OE | 00 | LU | C, 0 |
| C9 |  | Ret | 1 | C9 |  | Ret |  |

This will give you the expected result of 0 as $H L=0$ (both registers $H$ and $L$ have been set to 0 ) or $B C=0$, depending on which program you run.

## EXERCISE:

You might like to try a few fancy tricks, such as loading A with a number, transferring to $L$, setting $H$ to 0 and so on.

## EXERCISE:

ZX 80 users only : an interesting point to think about - what happens when you set $H$ to 200 and $L$ to 0 ?
$200 * 256+0=51,200$
You won't get the answer of 51,200 .
Why?

## FLAGS AND THEIR USES

Flags are those nice buntings you can wave on state occasions ... wrong!
In Machine Language, the word "Flag" implies "Indicator" - a flag is something you put up if you wish to indicate to someone else that a certain condition exists.

The obvious example is in boating where you rig up a flag to indicate distress, country, piracy or whatever.

The reason we use flags in machine language is to give the programmer information about the status of the number in the CPU's right hand (the - $A$ - Register) or information about the last calculation just performed.

You will remember that one of the $\mathrm{CPU}^{-s}$ registers is dedicated to be a Flags Register. You may also have noticed at the start of the last chapter a table summarising the various instructions to be discussed in that chapter, and that part of that table was devoted to the effect each instruction would have on the flags. (Fortunately none of the instructions discussed in the last chapter affected any of the flags).

The flag whose functioning is easiest to understand is the ZERU FLAG.
This flag will be run up the flag-pole if the contents of the " $A^{-}$register is zero.

There are many important decisions which will depend on whether " $A$ " is zero. Note that the zero flag is either on or off. You can ${ }^{-1}$ have an inbetween result (shade of 'a little pregnant ${ }^{-}$) so that you would only need one bit to define the zero flag.

The same is true for all the other flags as well. They are either on or off and require only one bit.

THE DIFFERENT KINDS OF FLAGS:
The " $F$ " register is a regular 8-bit register and could therefore accomodate 8 different flags. In practice however the designers could only think of 6 flags!


Actually the designers thought of seven flags, but decided that one bit could serve as both flags: the parity/overflow flag.

Let us now look at each of these flags in detail:
ZERO FLAG:
This is the flag we have already discussed above. Its application is obvious, and the flag is usually set after an arithmetic operation as it serves to indicate the contents of the " $A$ " register.


Note carefully however that it is possible to have the " $A$ " register contain 0 and for the zero flag not be set. This could easily happen by using the

$$
\text { LD } \quad A, 0
$$

instruction.
We have mentioned above that none of the 8 -bit load instructions had any effect on any of the flags.

The zero flag is also set if the result of the "Rotate and Shift" group of instructions results in a zero.

As well, the zero flag is the only visible result of some testing instructions, such as the "Bit Testing" group of instructions. In those cases the zero flag is put on if the bit tested is zero.

## SIGN FLAG:

The sign flag is very similar to the zero flag and operates on very much the same set of instructions (with the major point of departure being the "Bit Testing" group where the concept of a negative bit is somewhat meaningless in any case).

In the case of the sign flag, it will be set if the result of the arithmetic operation is negative.

## CARRY FLAG:

This is one of the more important flags available in assembly language, for without it the results of assembly language arithmetic would be totally meaningless.

The point to remember is that assembly language instructions always refer
to either 8-bit or 16-bit numbers.

This means that the numbers we are dealing with can be either :
8-bit $==>\quad 0-255$
16-bit $=\Rightarrow \quad 0-65536$
Consider the situation where we subtract 200

- 201

Result $=255!$
This is a direct consequence of only having a limited number range available, and the same thing can obviously happen with 16-bit numbers.

The carry flag can also be set by addition operations.
It is therefore convenient to think of the carry bit as the 9th bit of the " $A$ - register:

| No. | ${ }^{-}{ }^{-}$ | Number in Bit Form |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 132 | - | 10 | 0 | 0 | 0 | 1 | 0 |
| 135 | - | 10 | 0 | 0 | 0 | 1 | 1 |
| 267 | 1 | 00 | 0 | 0 | 1 | ) | 1 |

But as we do not have 9 bits, the " $A$ - register would contain the number "Decimal $11^{\circ}$ and the carry would be on (i.e. $=1$ ).

You can see that on subtraction borrowing from a 9th bit would leave a ${ }^{\text {1" }}$ there as well.

MACHINE LANGUAGE EQUIVALENT OF "IF ... THEN ...."
The equivalent in a basic program is:
If $\mathrm{A}=0$ then ...
where what follows can be "Let ...".
or "Goto ...".
58.

Exactly the same kind of decision can be programmed in Machine Language (except for the "Let ..."). Instead of saying "If $A=0$ ", we merely look at the zero flag: If it is on, then we know $A=0$.

The three flags we have been considering to date are in the main the only ones which allow us to execute a branch or a choice in the next instruction to be executed.

The format of such instruction is as follows:
For example:
JP CC, End
Where "JP" is the mnemonic for "Jump" and "tnd" is a convenient label. The instruction is read in English as "Jump on condition cc to end".

The condition "cc" could be any of :

| Z | $\Rightarrow$ Zero) |
| :---: | :---: |
| NZ | $\Rightarrow$ Not Zero) |
| P | $\Rightarrow$ Positive) |
| M | $\Rightarrow$ Minus) |
| C | $\Rightarrow$ Carry Set) |
| NC | $\Rightarrow$ No Carry) |

The other three flags tend not to be of so much use in every day programming. They are:

## PARITY / OVERFLOW FLAG:

This flag acts as the parity flag for some instructions, and as the overflow flag on others, but there is rarely any confusion as the two types of operations do not commonly occur together.

The parity side of it comes into effect during logical operations and is set if there is an even number of bits in the result. We deal with this in greater detail in the chapter on logical operations.

The overflow is a warning device that tells you that the arithmetic operation you have just performed may not fit into the 8 -bits. Rather than actually telling you that the result needed a 9th bit, this tells you that the 8 th bit changed as a result of the operation!

In the example above, adding 132 and 135 , the 8 th bit was " 1 " prior to the addition and ${ }^{-} 0^{-}$afterwards, so that the overflow would have been set. But the overflow would al so be set by adding:

| 64 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| ---: | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| + | 65 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 |  |  |  |  |  |  |  |  |
| - | - | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1

SUBTRACTION FLAG:
This flag is set if the last operation was a subtraction!

## HALF-CARRY FLAG:

This flag is set in a manner similar to the carry flag but only in the case of an overflow or borrow from the 5 th bit instead of fram the 9th bit!

Both the subtract flag and the half-carry flag are of use only in "Binary Coded Decimal" arithmetic, and we deal with these flags in the chapter on "BCD Arithmetic".

## COUNTING UP AND DOWN

In the last chapter we examined the concept of flags, and in the chapter before we found out how the CPU gets certain numbers onto its fingers and toes.

Let us now examine the simple possible way to manipulate numbers on one $s$ fingers: we can increase the number represented on our fingers or we can decrease the number represented.

This is a pretty rudimentary arithmetic, but it gets beyond loading specific numbers onto your fingers. The action of counting up is essentially: whatever number you have on your fingers,increase by one.

This can be used in such ordinary situations as census taking or monitoring the traffic at a particular intersection.

COUNTING UP
It is possible on the 280 to increase the count on the fingers of every single hand the CPU has. This is what we mean by the general mnemonic: INC $r$
"INC" is read in English as "Increase" and is therefore fairly selfexplanatory.

It is also possible to increase the count held on the toes of any of the feet (including the register pairs, which are not really feet, as we saw).

This increasing of the count on our toes is written as:
INC $\mathbf{r r}$
INC IX
INC IY

Where " rr " denotes a register pair, such as "BC", " $D E^{\prime}$, or " HL ".
Note again the simple way we have of denoting which operations are using 8-bit numbers and which are using 16-bit numbers:

The 8 -bit numbers are denoted by a single letter, while The 16-bit numbers are denoted by two letters.
But the "Counting Up" instruction is in fact even more powerful than this might indicate. It is possible to increase the count of any memory location if we are able to specify its address using the Index Registers or the "Favoured Register Pair", HL:

INC ( IX + d)
INC ( $\mathrm{IY}+\mathrm{d}$ )
INC (HL)
(Where " $d$ " is the displacement - not the Register!)
IMPURTANT NOTE:
Remember carefully our convention of reading brackets:
Brackets $={ }^{-}$Contents of ${ }^{-}$
This is very important as there is a lot of similarity between the instructions

INC HL
INC (HL)
But a world of difference in their execution.
The first would be read as "Increase HL" while the second would be read as "Increase the contents of the location whose address is H.". (This second reading is often abbreviated to "Increase the contents of HL".)

As long as you remember the rules of the menmonic abbreviations you will be saved from this kind of confusion. Let us examine how each operates, and let's assume that $\mathrm{HL}=16396$.

INC HL: Look at HL. Increase the count on its fingers by one. Result:
HL = 16397
INC (HL): Look at HL. Find the memory location referred to by this number. Increase the count in that location by one. Result:
HL $=16396$
$(16396)=(16396)+1$
These are significantly different operations. Note also that while -INC $\mathrm{HL}^{-}$is an instruction acting on a 16-bit number, "INC (HL) is an instruction which acts on an 8-bit number only - the number stored in location 16396!


## DECREASING THE COUNT:

The symmetrical nature of the 280 instruction set would almost certainly ensure that everything you can increase you can also decrease, and this is indeed the case:

DEC r
DEC rr
DEC IX
DEC IY
DEC (HL)
DEC $(I X+d)$
DEC ( $1 Y+d)$
The mnemonic "DEC" is read in English as "Decrease", and the same careful attention to the use of brackets must by applied here.

## EFFECT ON FLAGS:

Because the increase or decrease instructions which operate on 8-bit numbers affect every flag except the carry flag, this is a very good place to review the operation of the flags.
(Note that the increase and decrease instructions which operate on 16-bit numbers do not effect any of the flags!)

SIGN: This flag will be set $(=1)$ if bit 7 of the 8 -bit result is 1 .

2ERO: This flag will be set (=1) if the 8-bit result is zero.

OVERFLOW: This flag will be set ( $=1$ ) if the contents of bit 7 of the 8 -bit number is changed by the operation.

HALF-CARRY:This flag will be set ( $=1$ ) if there is a carry into or a borrow from bit 4 of the 8-bit number.

NEGATE: This flag is set if the last instruction was a subtraction. Thus it is not set ( $=0$ ) for "Inc", and set (=1) for "Uec".

## SUGGESTEU EXERCISES:

Use the "Load", "Inc" and "Dec" group of instructions to return the numbers you want as a result of the "USR operation.

This will give you familiarity with these instructions.

## INSTRUCTIONS FOR ONE-HANDED <br> ARITHMETICAL OPERATIONS

| MNEMONIC | BYTES | TIME TAKEN | $\begin{aligned} & \text { EFFECT } \\ & \text { C Z PV } \end{aligned}$ | ON FLAGS <br> S N H |
| :---: | :---: | :---: | :---: | :---: |
| Add Register | 1 | 4 | \# \# | \# 0 |
| Add Number | 2 | 7 | * \# | * 0 |
| Add (HL) | 1 | 7 | * \# | * 0 |
| Add ( $1 \times+d$ ) | 3 | 19 | * \# | \# 0 \# |
| Add ( $\mathrm{I} \mathrm{Y}+\mathrm{d}$ ) | 3 | 19 | \# \# | * 0 |
| ADC Register | 1 | 4 | * \# | * 0 |
| ADC Number | 2 | 7 | * \# | \# 0 |
| ADC ( HL ) | 1 | 7 | \#\# | \# 0 |
| ADC $(1 X+d)$ | 3 | 19 | \# ${ }^{\prime \prime}$ | \# 0 |
| ADC ( $1 \mathrm{Y}+\mathrm{d}$ ) | 3 | 19 | (1) | \# 0 |
| Sub Register | 1 | 4 | * \# | (1) |
| Sub Number | 2 | 7 | * \# | (1) |
| Sub (HL) | 1 | 7 | * \# | *1* |
| Sub (IX+d) | 3 | 19 | * \# | (1) |
| Sub ( $1 \mathrm{Y}+\mathrm{d}$ ) | 3 | 19 | \# \# | (1) |
| SBC Register | 1 | 4 | * \# | * 1 |
| SBC Number | 2 | 7 | ** | (1) |
| SBC (HL) | 1 | 7 | \#\# | \#1 |
| SBC ( $1 x+d$ ) | 3 | 19 | \#\# | (1) |
| SBC ( $1 \mathrm{Y}+\mathrm{d}$ ) | 3 | 19 | * \| | * 1 \# |
| CP Register | 1 | 4 | * \# | (1) |
| CP Number | 2 | 7 | 1 1 | (1) |
| CP (HL) | 1 | 7 | ** | \#1 |
| CP ( $1 \times+d$ ) | 3 | 19 | * \# | (1) |
| CP ( $1 \mathrm{Y}+\mathrm{d}$ ) | 3 | 19 | \#\#\# | \#1" |

[^0]One hand arithmetic is just our reminder that all of these operations in this chapter involve only 8-bits and all of them must be carried out through our right hand.

It seems that only our right hand knows how to add or subtract!
This fact is so ingrained in the 280 machine language menmonics that the abbreviation " $A$ - is even omitted. For example to add " $B^{-}$" to ${ }^{-} A^{-}$, we would normally expect to see ADD A,B
But in fact the mnemonic is
ADD B.
Despite this limitation on arithmetical instructions, the 280 language is very versatile in what we can actually add to whatever number we have on our right hand:

Add $r \quad$ Add any single register to $A$
Add $n \quad$ Add any 8-bit number to $A$
Add (HL) Add the 8-bit number in the box whose address is given by HL
Add $(I X+d)$ Add the 8-bit number in the box whose address is given by $I X+d$
Add (IY +d) Add the 8-bit number in the box whose address is given by IY+d

You can appreciate that this is an extremely versatile range of possible numbers we can add to whatever number is stored in $A$ - any number, any register and virtually any way we care to define a memory location.

The one that is missing is
Add (nn)
where we define the address in the course of the program.

As a result the only way to get such an instruction would be to write: LD HL, nn
ADD (HL)
Note also the favoured role of the HL register again. We cannot specify the memory location using the BC or DC register pairs.

The other limitation implicit in all this is also the limitation of 8-bit numbers:

LD $\mathrm{A}, 80 \mathrm{H}$
ADU 81 H
will give a result of only 1 in " $A^{\circ}$ but the carry flag will be set to indicate the result did not fit in.
(If the hexadecimal arithmetical confuses you, it's really just the same as ordinary arithmetic but you go to ${ }^{\prime} F^{\prime}$ instead of stopping at ${ }^{-9} 9^{\prime \prime}$ :

80

```
+81
101 H as \(8+8=16=10 \mathrm{H}\) )
```

There is therefore the very useful instruction "ADC" which we read as "ADU WITH CARRY".

This is exactly the same as the "ADD" instruction, with the same range of numbers which can be added to ${ }^{\prime} A^{\prime}$, except that the carry is added on (if it is set).

This makes it possible to add numbers greater than 255 together, by a chaining operation:
E.G. To add 1000 (i.e. U3E8H ) to 2000 (i.e. 0700 H ) and store the result in BC:

| LD A,E8H | ; Lower Part 1st No. |
| :--- | :--- |
| ADD $D O H$ | ;Lower Part 2nd No. |
| LD $C, A$ | ;Store Result in C |
| LD A,03H | ;Higher Part 1st No. |
| ADC $07 H$ | ;Higher Part 2nd No. |
| LU B,A | ;Store Result in B |

After the first addition (E8 + DO ) we will have the carry set (because result was greater than FF ) and A containing B8 (check this for yourselves!).

The second addition ( $3+7$ ) will yield not UAH ( $=10$ Uecimal) as might seem on the surface but $O B H$ ( = 11 Decimal) because of the carry.

The final result is therefore $O B B 8 H=3000!$ This chaining could go on to take care of any size number rather than simply in a register pair.


This is exactly the same as 8 -bit addition. Two sets of commands exist, one for ordinary subtraction, and one for subtraction with carry:

SUB $s$ - SUBTRACT S
SBC s - SUBTRACT S WITH CARRY
The notation " $S^{\text {" }}$ is meant to denote the same range of possible operands as for the Add instruction.

## COMPARING TWO 8-BIT NUMBERS:

Let us step back from machine language for a moment and consider exactly what it is we mean when we compare two numbers:

We know what happens when the two numbers being compared are the same they are "equal". One way to denote this in an arithmetical format would be to say that the difference between the two numbers was zero.

What if the number being compared is greater than the first number (comparison does imply relating two numbers: we compare a number with what we already have on our fingers). Then the result after subtracting the new number will be negative.

Similarly if the new number is smaller, then the difference will be positive.

We can use these concepts to devise a system of comparisons in machine language. All we need are the flags and the subtract operation. Suppose we wish to compare a range of numbers with 5 , say:

$$
\begin{array}{ll}
\text { LD A,5 } & \text {;Number we have } \\
\text { SUB N } & \text {;Number being compared }
\end{array}
$$

Then we will have the following results -
If $N=5 \quad$ Zero Flag set, Carry flag not set
If $\mathrm{N}<5 \quad$ Zero Flag not set, Carry not set
If $N>5$ Zero Flag not set, Carry flag set.
It is therefore clear that the test for equality will be the zero flag, and the test for ">" will be the carry flag. (The test for "く" is the absence of both flags).

The only inconvenience of this method is that the contents of " $A$ " have been altered by the operation.

Fortunately we have the "CP s" operation. This is read in English as "Compare". Note that it can only compare what we already have in the " $A$ " register; the range of possible numbers to be compared are the same as for addition.
"Compare" is exactly the same as "Subtract" except that the contents of " $A$ - are unchanged. The only effect is therefore on the flags.

## INSTRUCTION FOR TWO-HANDED

 LOADING OPERATIONSMNEMONIC
BYTES
TIME TAKEN

| LD Reg Pair, Number | 3 | 10 | - | - | - | - | - | - |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| LD IX, Number | 4 | 14 | - | - | - | - | - | - |  |
| LD IY, Number | 4 | 14 | - | - | - | - | - | - |  |
| LD (Address), BC or DE | 4 | 20 | - | - | - | - | - | - |  |
| LD (Address), HL | 3 | 16 | - | - | - | - | - | - |  |
| LD (Address), IX | 4 | 20 | - | - | - | - | - | - |  |
| LD (Address), IY | 4 | 20 | - | - | - | - | - | - |  |
|  |  | 4 | 20 | - | - | - | - | - | - |
| LD BC or DE, (Address) | 3 | 16 | - | - | - | - | - | - |  |
| LD HL, (Address) | 4 | 20 | - | - | - | - | - | - |  |
| LD IX, (Address) |  | 20 | - | - | - | - | - | - |  |

## FLAGS NOTATION:

```
* Indicates flag is altered by operation
O Indicates flag is set to 0
1 Indicates flag is set to 1
- Indicates flag is unaffected
```



## MANIPULATING NUMBERS

## WITH TWO HANUS

In the preceding chapters we have seen just how agile the CPU can be in manipulating numbers on one hand.

His mathematical ability is such that he can also perform very complex calculations involving large numbers with only one hand.

But there are points where it it impossible to specify everything one wants with just 8-bit numbers. If we were limited to just the range of 0 - 255 of the 8 -bit numbers our computer would indeed be a very limited machine.

The most glaring example of needing l6-bit numbers is specifying the address of a memory location. We implied that such a manipulation would be possible when we discussed instructions such as LD A,(HL).

The slow way of doing things would be to load each individual register in the register pair, as we did in the exercises of Chaper 7.

Fortunately for us there are some (but only a few) instructions on the 280 chip which allow us to manipulate 16 -bit numbers. In this chapter we shall be dealing solely with loading 16-bit numbers, while the next chapter will deal with 16-bit arithmetic.

SPECIFYING ADDRESSES WITH 16-BIT NUMBERS:
Please note that all addresses must be specified by a 16-bit number.
You just can't specify an address with only 8-bits, even if it is only addresses from 0 to 255. The way the CPU works, it's not an address unless it is 2 bytes of 8 bits each.

We implied this when we used the short shorthand of LD A, (NN)

So also remember that 16-bits numbers are stored in register pairs high number first (check again with Chapter 5. - "HL" stands for "High"; "Low").

## STORING 16-BIT NUMBERS IN MEMORY:

There is one facet of $\mathbf{Z 8 0}$ design which is very difficult to explain or justify:

When loading 16 -bit numbers into memory, the reverse convention from that of register pairs is used.

The low bit is always stored first in memory.
Let us consider a situation where we place the contents of HL into memory:

BEFORE:
H L
0102

LOCATION
17100
17101
17102

CONTENTS
00
00
00

Let us assume that HL contains the number 258 decimal $=0102 \mathrm{H}$. The memory locations are all empty.

AFTER:
LOCATION
CONTENTS
17100
02
H L
17101
01
1710200

The convention with 16-bit numbers stored in memory (and in program listings) is that the low bit is always stored first.

There is no justification for that decision except to say that this was what the designers of the 280 came up with and we now have to live with it.

Please be sure to read this carefully and make sure that you are familiar with this reversal of convention. It is likely to be the single most important source of errors in programs:

In registers: high bit stored first
In memory and programs: low bit stored first.
It is not something that can be glossed over and ignored as every time you deal with a l6-bit instruction in machine code you will need to think carefully about the order of the low and high bits.

Do not however feel put off by this - life on the 280 would be virtually impossible without 16 -bit instructions and it's a price we have to pay.

LOADING 16-BIT NUMBERS:
The 16 -bit load group at its simplest comprises of loading a 16-bit number in the register pair. The general mnemonic abbreviation is

LD rr, nn
Once again we are using the notation of 2 letters to indicate a 16-bit number. "rr" means any register pair, "nn" any l6-bit number.

For those of you without the benefit of an assembler - that is if you have to convert the memonics into code by hand using the tables at the back of the book - then the discussion we had of the order of the 16-bit numbers in memory becomes crucial.

Even if you do have an assembler, you should be aware of these reversals of order to enable you to "read" the code when peeking into memory.

Let us look at a specific example:
Load HL with 258
the memonic for this is
LD HL,0102H
The instruction for "LD $H, \mathrm{nn}^{\text {- }}$ is, as you will find at the end of the book,
$21 X X X X$
This means that the number $0102 H$ needs to be inserted in place of the ${ }^{-} X X$ $X X^{-}$. But because of the reversal rule, we do not enter this as 0102H.

The proper instruction is therefore:
210201
In our examples we will show you this as
210201
LD HL, 0102H ( = 258)

You may not have problems entering our programs, but you need to be familiar with this when you write your own programs.

OTHER 16-BIT LOAD INSTRUCTIONS:
As well as being able to load 16 -bit numbers directly into the register pairs we can also load 16 -bit numbers directly into the index registers (which are both 16-toe feet, as you will remember).

LU IX, nn
LU IY, nn
We can also manipulate information between a register pair and two successive locations in memory. (This is the 16-bit equivalent of loading the information from a single register into a single memory location).

The general instructions are
LD (nn), dd
LD (nn), IX
LD (nn), IY
Remember that brackets are the shorthand for "Contents Of", so that the last instruction would be read as "Load the contents of memory location nn with register IY".

Because we are dealing with 16-bit numbers, we are actually loading the memory location specified and the following memory location into the register pair. It is not necessary to specify both addresses (because the CPU can figure out the address of the second location) but be careful not to confuse 8 -bit operations with 16 -bit operations.

The reciprocal nature of many of the instructions is also apparent here, and we can also load a register pair of index register with whatever is in a specific pair of memory locations:

LU dd, (nn)
LD IX, (nn)
LU IY, (nn)

## EXERCISE:

2X80 version: run the following short program entering it through the editing program -

```
2A OC 40
C9
LD HL, (16396) RET
```

We know from the $2 \times 80$ manual that 16396 and 16397 contain the address for the start of the screen display. If you now "RUN" this program by entering

Start for USR? 17300
(assuming you have loaded it at 17300), you will receive as an answer the address of the display start.

Now try running the following program:
2A OE 40
LD H., (16398)
C9 RET

This will give you the address at the end of the screen. Is this what you expected? Can you work out why the screen is only $\mathbf{2 5}$ characters long?

NOTE VERY CAREFULLY THAT THE NUMBERS ARE ENTERED LOW BYTE FIRST ANU YOU WOULD GET A TOTATIY ERRUNEOUS ANSWER IF YOU WERE TU ENTER THEM THE OTHER WAY ROUND.

## ZX81 VERSION:

In the $\mathbf{Z X 8 1}$ case the screen start is also defined by the contents of memory locations. 16396 and 16397 but this time we want the result to be returned in register pair " $B C^{\prime}$ :

| ED $4 B$ | $0 C$ | 40 |
| :--- | :--- | :--- |
| $C 9$ |  | LD BC, (16396) |

In the $2 \times 81$, we know that once the program is finalised the position of the screen start is fixed and we only need to determine this once in each program.

On the other hand, if the system does not have a minimum of 3-1/4K of memory, the locations where the variables are stored will move around and the start of the variable file can be found by
ED $48 \quad 10 \quad 40$
LD BC, (16400)
C9
RET

Note that "LD BC, (nn)" is a four-byte instructionl

## MANIPULATING THE STACK

You may recall the image we developed in the beginning of the book of the stack where the CPU was able to keep information without having to remember the address of that particular information.

One of the advantages, possibly inadvertent, of the stack operations is that we can only PUSH and POP information in 16 -bit lots. This is because the stack is primarily designed to remember addresses and we need to specify addresses as 16-bit numbers.

The general instructions for pushing information to the stack are
PUSH rr
PUSH IX
PUSH IY
And the general instruction for popping information back from the stack are

```
POP rr
POP IX
POp IY
```

This is an exceptionally simple instruction, and you will note the lack of need to specify an address.

For the ordinary register pairs - i.e. not the index registers - these instructions are only a single byte long and therefore very economical in terms of programming space.

PUSH instructions are also not destructive: that is, the 16-bit register still contains the same information after the PUSHES.

Note that because we can PUSH any register pair and POP any register pair, the register you PUP may not be the same as the one you PUSHEU!

For example
PUSH BC
POP HL
The effect of these two instructions is to leave the contents of the BC register unchanged but set the HL register to whatever the contents of the $B C$ register were at the time of the push instruction.

This effectively adds an instruction of the type
LD rr, rr'
from the 16-bit load group which was conspicuously missing. As each of the PUSH and POP instructions for the register pair is only one byte long, the cost in terms of memory is not expensive.

The other extra is that we are able to PUSH or POP the register pair AF! This is one of , the few instructions where AF is treated as a register pair, but it is obviously sensible because there are many times when we would like to preserve the contents of the flags.

## MOVING THE STACK AROUND:

As you know, the real strength of the PUSH and POP instructions is that we do not have to think about the addresses.

But you will agree that it does not necessarily make sense that the same area of memory should serve as a stack if you have 16 K of memory as if you only have 1K.

The way the CPU actually keeps track of the address of the stack is by means of a "stack pointer", wheih can be thought of as a $\mathbf{1 6 - b i t}$ register. We did not include it in our discussion of registers because it is not a register that can be manipulated in the same manner as the other registers.

The main thing one would want to do with the stack pointer is to define its position in memory, and that is exactly the type of instruction that is avallable.

INSTRUCTION FOR
STACK OPERATIONS

| MNEMONIC | BYTES | TIME |  | EFFE |  | ON | FLAGS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TAKEN | C | 2 | PV | 5 | N H |
| PUSH Reg Pair | 1 | 11 | - | - |  |  |  |
| PUSH 1X or iY | 2 | 15 | - | - | - | - | - - |
| POP Reg Pair | 1 | 10 | - | - | - | - | - - |
| POP 1X or 1Y | 2 | 14 | - | - | - | - | - - |
| LD SP, Address | 3 | 10 | - | - | - | - | - - |
| LD SP, (Address) | 3 | 20 | - | - | - | - | - - |
| LD SP, HL | 1 | 6 | - | - | - | - | - - |
| LD SP, IX or IY | 2 | 10 | - | - | - | - | - - |

## FLAGS NOTATION:

* Indicates flag is altered by operation

0 Indicates flag is set to 0
1 Indicates flag is set to 1

- Indicates flag is unaffected


81. 

| LD | $S P$, | $n n$ |
| :---: | :---: | :---: |
| LD | SP, | $(n n)$ |
| LD | $S P$, | $I X$ |
| LD | $S P$, | $I Y$ |

You can examine the stack of the Sinclair $2 \times 80$ and $2 \times 81$ by using the editing program, and looking in the last 30-40 bytes from the top of your memory.
"** Do not change the contents of the locations in the stack**"
Almost any change will cause your Sinclair to crash - the screen will go black and you wil have to turn the power on again. This is because the operating system places a lot of information it requires on the stack and changes will cause it to bomb.

For the same reason do not try to manipulate the position of the stack pointer unless you are sure of what you are doing.

## NOTE:

In a well organised program the number of POPs and PUSHes should end up the same no matter which path the program follows. Any miscalculation may lead to funny results.

Note also that whenever a subroutine is called, the return address is pushed on to the stack. We can therefore use this to examine the address at which the USR subroutine is called by means of the following program:

2X80 Version:
POP HL ; get address in HL PUSH HL ; put it back on stack RET

2X81 Version:
POP BC ; get address in BC PUSH BC ; put it back on stack RET

One of the benefits of being able to have 16-bit capabilities on what is effectively an 8-bit processor is that we can use the lb-bits to specify addresses, or to perform calculations involving integer numbers up to about 64,000 (or in the range - 32,000 to $\mathbf{+ 3 2 , 0 0 0}$ if negative numbers are to be permitted).

In this light it is easy to see why the original Sinclair $2 \times 80$ limited all numbers to integers and to the range - 32,000 to $+32,000$.

But even though we can perform some arithmetic with two hands, our title for this chapter gives a hint of what is to come - two handed arithmetic is a little clumsy compared to one-nanded arithmetic. The range of options is just not there!

## FAVOURED REGISTER PAIR:

In the same way that the " $A$ " register is the favoured register in 8 -bit arithmetic, so there is a favoured register pair in 16-bit arithmetic, and it is the "HL" register pair.

This favoritism is not quite so pronounced as in the 8-bit case, so we do not omit the name of the register pair.

## ADDITION:

The additions are quite straightforward:
ADD HL, BC
ADU HL,DE
ADD HL,HL
ADD HL,SP
But that is it!

Note that it is not possible to add an absolute number to HL - e.g. "Add $\mathrm{H}, \mathrm{nn}^{-}$is not permitted. To perfom that kind of calculation we need to:
$L D$
ADE HL
HL, DE

When you consider that this now ties up four of the 8-bit registers out of a total of 7 , you realise it's not something you want to do too often.

Note also that there is no addition between "HL" and the index registers. You will also remember that there is no load instruction which permits you to transfer the contents of $I X$ or IY to $B C$ or $D E$, so the only way to do such an additon would be like:

| PUSH | $1 X$ |
| :--- | :--- |
| POP | DE |
| ADD | $H L, D E$ |



## INSTRUCTIONS FOR

TWO HANDED ARITHMETIC

| MNEMONIC | BYTES | $\begin{aligned} & \text { TIME } \\ & \text { TAKEN } \end{aligned}$ | EFFECT ON |  |  |  | FLAGS |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | C | Z | PV | S |  |  |
| ADD HL, Reg Pair | 1 | 11 | * | - | - | - | 0 | ? |
| ADD HL, SP | 2 | 11 | * | - | - | - | 0 | ? |
| ADC HL, SP | 2 | 15 | + | \# | \# | \# | 0 | ? |
| ADD IX, BC or DE | 2 | 15 | * | - | - | - | 0 | ? |
| ADD IX, 1X | 2 | 15 | * | - | - | - | 0 | ? |
| ADD IX, SP | 2 | 15 | * | - | - | - | 0 | ? |
| ADD IY, BC or DE | 2 | 15 | * | - | - | - | 0 | ? |
| ADD IY, IY |  | 15 | * | - | - | - | 0 | ? |
| ADD IY, SP | 2 | 15 | \# | - | - | - | 0 | ? |
| SBC HL, Reg Pair | 2 | 15 | * | * | \# | * |  | $?$ |
| SBC HL, SP | 2 | 15 | * | \# | \# | * | 1 | $?$ |

## FLAGS NOTATION:

* Indicates flag is altered by operation

0 Indicates flag is set to 0
1 Indicates flag is set to 1

- Indicates flag is unaffected
? Indicates effect is not known

The one point of note is the "SP" register - the stack pointer.This is one of the very $f e w$ operations where " $S P^{\prime}$ is treated like a register proper, but obviously you can ${ }^{-t}$ use it as a variable! Think of what would happen to all the pops and pushes if you varied the contents of " $S P^{\text {" at will. }}$

## EFFECT ON FLAGS:

l0-bit arithmetic is where the carry flag really comes insto a field of its own, because as you can see from the table at the beginning of this chapter, the only other flag that is affected by the "ADD" instruction is the "subtraction" flag (and all we are saying is that the "AUD" instruction is not a subtraction!)

The carry flag will be set if there is an overflow from the high bit of ${ }^{\prime} H^{\prime}$ ( - any overflow from " $L$ " is automatically placed into ${ }^{-} H^{-}$by the calculation).

ADD WITH CARRY:
Because of the limited nature of l6-bits, we are able to chain additions just as in the 8-bit case. The instruction "Add with Carry" - mnemonic "ADC" operates in a similar manner to "add" and with the same range of register pairs:

ADC HL,BC
ADC HL,DE
ADC HL,HL
ADC HL,SP
16-BIT SUBTRACTION:
16-bit subrtraction is also a very straightforward operation, but there is no subtraction without carry: if you are not sure of the status of the carry flag, be sure that your program includes a line to clear the carry flag before any subtraction operation.

SBC HL,BC
SBC HL,DE

```
SBC HL,HL
SBC HL,SP
```

(That last instruction has obvious application: set " HL " to the end of the memory used by your program, screen display and variables, subtract "SP", and the result <negative> will be the amount of free space. Can you write a simple program to do that? See the end of the chapter to confimmour solution).

## EFFECT OF CARRY ARITHMETIC ON FLAGS:

You may have noticed that three other flags are affected by the "Add with Carry" and "Subtract with Carry" that were not affected by the simple 16bit addition instructions.

These are the zero flag, the sign flag and overflow flag. Each of these is set according to the result of the operation.

## INDEX REGISTER ARITHMETIC:

Index registers are totally limited to addition without carry!
Furthermore the range of registers that can be added to the index registers is extremely limited:

> Adding the " BC " or "UE" register pair Adding the index register to itself Adding the stack pointer.

## SOLUTION TO MEMORY LEFT EXERCISE:

The end of the memory space the program uses is defined by the contents of the E-line memory location. These are different for the $2 \times 80$ and $2 \times 81$ :

ZX80 E-line is in 16394,16395
ZX81 E-line is in 16404,16405
Obviously if we load H. with the contents of that location we are halfway there:

LU HL, (E-line)
then subtract the "stack pointer":
SBC HL,SP
Because of the "carry" we need to clear the carry flag. This is most easily achieved by the "AND $A^{-}$instruction, which is covered later in the book. Three-quarter marks if you knew you had to allow for the carry but didnt know how to do it. One-quarter marks if you forgot all about the carry.

Because the stack pointer is in higher memory than the top of your progran (or else you are in diabolical trouble) the result will be negative.

Let us now proceed to get the number of bytes left as a positive number, using the " BC - register (" VE - would be just as good for this). We first want to shift HL to BC, but there is no "load instruction to do this and we will need to use a push followed by a pop:

PUSH HL
POP BC
HL still has the same information as before, so $H L=B C$.
To get HL=-BC, subtract BC from HL twice (but don ${ }^{-1}$ forget that the carry has just been set by the subtraction so must be cleared again):

AND A
SBC HL,BC
SBC HL,BC
HL now contains the negative value of what it contained betore - i.e. the positive number of bytes left.

```
ZX81 users will now need to get the number into the "BC" register pair
again to get a result from the "USR" function. To get "HL" back into
"BC':
                                    PUSH HL
                                    POP BC
and finally a return from the USR function:
                                    RET
Did you get this right?
```

INSTRUCTIONS FOR LOGICAL OPERATORS

| MNEMONIC | BYTES | TIME | EFFECT |  |  | $\begin{gathered} \text { ON FLAGS } \\ \text { S } \mathrm{N} \text { He } \end{gathered}$ |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TAKEN | C | Z | PV |  |  |  |
| AND register | 1 | 4 | 0 | , | * | * | 0 | 0 |
| AND number | 2 | 7 | 0 | - | , | * | 0 | 0 |
| AND (HL) | 1 | 7 | 0 | + | 1 | * | 0 | 0 |
| AND ( $\mathrm{IX}+\mathrm{D}$ ) | 3 | 19 | 0 | + | - | * | 0 | 0 |
| AND ( $\mathrm{I} Y$ + D) | 3 | 19 | 0 | + | * | * | 0 | 0 |
| OR register | 1 | 4 | 0 | * | * | * | 0 | 0 |
| OR number | 2 | 7 | 0 | , | * | * | 0 | 0 |
| OR (HL) | 1 | 7 | 0 | * | * | * | 0 | 0 |
| OR (IX + D) | 3 | 19 | 0 | + | * | * | 0 | 0 |
| OR (IY + D) | 3 | 19 | 0 | \% | * | * | 0 | 0 |
| XOR Register | 1 | 4 | 0 | * | , | \# | 0 | 0 |
| XOR Number | 2 | 7 | 0 | + | 1 | + | 0 | 0 |
| XOR (HL) | 1 | 7 | 0 | + | , | * | 0 | 0 |
| XOR (IX + D) | 3 | 19 | 0 | + |  | + | 0 | 0 |
| XOR (IY + D) | 3 | 19 | 0 | + | \% | + | 0 | 0 |

## FLAGS NOTATION:

* Indicates flag is altered by operation

0 Indicates flag is set to 0
1 Indicates flag is set to 1

- Indicates flag is unaffected.


## LOGICAL OPERATORS

There are three operations which are as valuable in the field of machine (or assembly) language programming as the more commonly used ${ }^{+}{ }^{\circ}$, "-", multiplication or division. These are generally referred to as boolean operators after the man wo formulated the rules of these querations. These operations are:

AND
OR
XUR
We are already familiar with the concept of operations which apply to an entire number, but the reason that these operations are so valuable is they operate on the individual bits of the number.

Let us look at one of these operations, "And":

| BIT A | BIT B | RESULT BIT A AND BIT B |
| :--- | :--- | :---: |
|  | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

It is obvious that the result of an "AND"operation is to give us a " ${ }^{\text {- }}$ only if A ANU B both contained a ${ }^{*} 1^{\prime}$.

You may be asking yourself - "What is the point of such an operation?"
The "And" operation is extremely useful in that it allows us to mask a byte so that it is altered to contain only certain bits:

If for example, we wish to limit a particular variable to the range of 0 7 only, we quite clearly wish to indicate that we want only the bits $0-2$ to contain information. (If bit 3 contained information, the number would be at least 8 ).

```
E.g. 0
<------------>
These bits
must be "0".
```

If we therefore take a number whose value we do not know and apply the -and ${ }^{-}$operation with ${ }^{-7}$ ", the result will be a number which lies in the range 0-7.
E.g.

| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | $=10$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |


| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |$\quad \Rightarrow 7 \Rightarrow$ Mask

Result of and

Note that the $Z 80$ chip only allows for the "AND" operation to take place with the " $A^{-}$register. " $A^{-}$can be "AND"ed with a value, any of the other 8-bit registers or with (HL).
E.g. AND 7 Note that as only the " $A$ "

AND E register can be acted on,
AND (HL) it need not be mentioned in the instruction.
The same is true for the other Boolean operations, ${ }^{-} O R^{-}$and ${ }^{-} X U R^{-}$.
The "OR" operation is very similar in concept to the "ANU" operation:
BIT A BIT B BIT A ${ }^{-}$OR $^{-}$BIT B

| 0 | 0 | 0 |
| :--- | :--- | :--- |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

It is obvious that the result of an ${ }^{-} \mathrm{OK}^{-}$operation is to give us a ${ }^{-1}$ - if either $A$ or $B$ contained $a^{-1} 1^{-}$.

Again you may be asking what is the point of such an operation.
The "UR" operation is also extremely useful in that it allows us to set any bits in a number: if, for example, we wished to ensure that a number was odd, then quite clearly we have to set bit 0 . (The same result could be obtained by using the " SET $^{\text {- }}$ instruction).

## LD A, number

OR 1 ;make number odd
The above two lines would be a typical mnemonic listing.

The concept of "XOR" - pronounced Exclusive or" - is also easy to understand but its actual use in programming is more limited.
The result of " $X O R^{-}$is a ${ }^{-1} 1^{\text {- }}$ only if one of $A$ or B contains $\mathrm{a}^{-1} 1^{\text {- }}$.
In other words, the result is the same as for the "or" operation in all cases except when both $A$ and $B$ contain $a^{-1} 1^{-}$.

XOR => OR - AND
BIT A
BIT B
BIT A ${ }^{-}$XOR $^{-}$BIT B
0
1
1
0

The last thing we must consider is the effect that these operations have on the flags.

| ZERO FLAG | This flag will be on (=1) if the result is zero |
| :---: | :---: |
| SIGN FLAG | This flag will be on (=1) if bit 7 of result is set |
| CARRY FLAG | Flag will be off $(=0)$ af ter "AND", ${ }^{\circ} \mathrm{OR}^{-}$, ${ }^{-} \times \mathrm{XR}^{-}$ i.e carry will be reset. |
| PARITY FLAG | This flag will be on (=1) if there is even no. of bits |
| (Note that this | in the result: $1,0 \Rightarrow$ of |
| flag also doubles | $\begin{array}{llllllllllll}0 & 1 & 1 & 0 & 1 & 1 & 1 & 0\end{array} \Rightarrow$ of $f$ |
| as Overflow Flag) | $\begin{array}{llllllllll}0 & 1 & 1 & 0 & 1 & 0 & 1 & 0\end{array}$ |
| HALF-CARRY FLAG | Both flags turn of $\left.\mathrm{f}^{( } \mathbf{(}=0\right)$ |
| SUBTRACT FLAG |  |
|  | ${ }^{-3 C D}{ }^{-}$arithmetic. |

There is a special case of the Boolean operators which is very handy - the case of the register $A$ operating on itself.

AND A A is unchanged, carry flag cleared
OR A A is unchanged, carry flag cleared
$X O R A \quad A$ is set to 0 , carry flag cleared:
These instructions are of ten popular because they require only one byte to do what might otherwise require two. (Such as LU A,O).

The carry flag of ten needs to be cleared - e.g. as a matter of routine before using any of the arithmetic operations such as ADC Add with carry SBC Subtract with carry.

## LUUPS AND JUMPS

Loops and Jumps is what gives a computer program real power. Unce you have the ability to make decisions and to execute different bits of the programs as a result of previous calculations you are really getting places.

This freedom can also cause problems, create programs which are difficult to follow, and almost impossible to debug.

I would strongly suggest that you designed your computer programs carefully before entering code, and that is why we have included the chapter "Planning your Machine Language Program". I emphasise this now because loops and jumps are what will entice you away fron good program design.

## MACHINE LANGUAGE EQUIVALENT UF "GUTO":

In BASIC, you are familiar with the instruction "GOTU", whidh transfers control of your program to the instructions in the line you "GUTO".

Nothing could be simpler to implement in machine language: just specify the memory location you would like to CPU to find the next instructions and you are half-way there.

The most simple instruction is "Jump To":
JP XX XX
JP (HL)
JP (IX)
JP (IY)
one of these instructions can also be made ta be dependent on the status of one of the flags, such as the carry flag. This conditional Jump instrtuction is:
JP CC, NN
where CC is the condition to be met. If we had JP 2,0000
for example, this would be read "Jump" if zero flag is set to address ${ }^{-} 0000^{-}$. (This is the address the Sinclair jumps to when you turn the power on, and as such a "JP" to zero might be used in a machine language program if you wanted to clear all the memory and start again with ${ }^{\prime} \mathrm{K}^{\prime}$ ).

Now note that the CPU does not allow for any mistakes. If you say "Jump", it will jump. Because almost any code can be construed as an instruction, the CPU does not care if you land it in the middle of data, or in the second byte of a two-byte instruction: it will read the byte at the address it finds and presumes that is the start of the next instruction.

The way the CPU works out the "Jump" instructions is really quite simple: it has a little counter called the "Program Counter" which tells it where to find the next instruction to be executed. In the normal course of programming (that is, without jumps) the CPU looks at the instruction to be executed and adds however many bytes there are to the instruction to the program counter.

Thus if it meets a 2-byte instruction, it adds 2, while a 4-byte instruction will make it add 4 to the program counter.

When it comes across a "Jump" instruction, it merely replaces the contents of the program counter with whatever value you have specified. That is why you cannot allow any errors to creep in.

LONG JUMPS AND SHORT JUMPS:
We can describe the above instructions to be the machine language equivalent of a "Long Jump" because the l6-bit address allows us to jump to anywhere the Z80 chip can possibly 90.

The disadvantage of the long jump is that:
A. Uften we don ${ }^{-} t$ want to jump that far but still have to use a 3-byte instruction.
B. We cannot easily relocate the program to another part of memory because we are specifying the absolute address.

It was mainly to overcome these two disadvantages that the "Short Jump" was introduced. This is referred to as a "Relative Jump" and allows us to jump up to +127 bytes from our present position or up to -128 bytes from the present position. i.e. the distance jumped can be specified in one byte!

## RELATIVE JUMP INSTRUCTION:

The instruction mode is simple:
JR d
where $d$ is the relative displacement. We can also make the relative jump dependent on some. condition, such as whether the carry is set, or the zero flag is set, for example, these conditional jumps are written as

JR CC, d
where cc is the condition to be met.


The value of the displacement is added to the "Program Counter".
This means it takes the present value of the program counter and adds the relative value you have specified. The value you specify can be either positive - jumping forward - or negative - jumping baclwardst If you check back to our chapter on negative jumps you will realise this means that relative jumps are limited to the range -128 to +127 .

Note that, when the CPU is executing a relative jump instruction, the program counter is already pointing to the next instruction which would be executed if the condition was not met.

This is because when the CPU comes across "JR" it knows that it has a 2byte instruction to deal with and adds 2 to the program counter - the program counter is therefore pointing to the instruction after the relative jump!
E.g. In a program such as

| LOCATION |  | CODE |
| :--- | :--- | :--- |
|  |  |  |
| 17100 |  | Add A,B |
| 17101 |  | JR $2,02 H$ |
| 17103 |  | LD $B, 0$ |
| 17105 | Next | LD H.,4000H |

The following is the way the CPU deals with the program:
Load byte at 171000
Byte is part of l-byte instruction so set program counter to 17101
Execute instruction
Load byte at 17101
Byte is part of 2-byte instruction
so set program counter to 17103
Get next byte to complete instruction
Execute instruction
Load byte at 17103
Byte is part of 2-byte instruction
so set program counter to 17105
Get next byte to complete instruction
Execute instruction

Now this is the part where the relative jump instruction has to decide what to do about the program counter:

If the zero flag is set, add 2 to the program counter $\Rightarrow 17105$
If the zero flag is not set, do nothing $($ program counter $=17103)$

This also explains why there are two times shown for the time taken for this instruction. It takes less time to do nothing than to calculate the new program counter.

The CPU will therefore execute either the instruction at 17103 or the instruction at 17105 depending on the zero flag.

It is also possible to make the relative jump negative as we have already mentioned.

## EXERCISE:

Because the relative jump is a 2-byte instruction, and the program counter is pointing to the next instruction after the relative jump, what would be the effect of an instruction which read: JR -2

MACHINE LANGUAGE "FOR ...NEXT" LOOPS:
You are, I am sure, familiar with the "BASIC" form of the "FOR ...NEXT" loop:

```
    FOR I=1 to 6
    LET C = C+1
    NEXT I
```

The machine language equivalent is similar but takes a different form. Let us consider how we could implement the machine language loop using the arithmetic functions and the relative jump:

|  | LD B,1 | : Set Counter to 1 |
| :--- | :--- | :--- |
| Loop | LD A,7 | Max. of Counter + |
|  | INC C | : $=C+1$ |
|  | INC B | Increment Counter |
|  | CP B | is $B=A ?$ |
|  | JR NZ,Loop | if not loop again |

This will work, but note the following: We are tying up 2 registers, one to increase, and one to hold the maximum; and the instruction which increments the counter does not set any flags on completion.

A much better way would be if we counted down!
We know that we have to do the loop 6 times, so why not set ' $B$ ' to 6 and count down?
This will give us:

|  | LD B, 6 | Set Counter |
| :--- | :--- | :--- |
| Loop | INC C | C $=C+1$ |
|  | DEC B | Decrease Counter |
|  | JR NZ, Loop | Loop if not finished |

You can see that this is a much more efficient way of doing things.
The $2 \times 80$ chip has a special instruction which combines the
last two lines above.
This instruction is written as:
DJNZ d
And is read as "Decrease (B) and Jump if Not Zero". (The $d$ is the relative displacement). This instruction is a 2-Byte instruction and therefore saves one byte on the above coding.

Because of the existence of this special instruction, the ' $B$ ' register is usually used as a counting register.

The limitation of 'DJNZ' instruction is that one can only count up to 256.

DJNZ instructions can however be nested, if required:

|  | LD B,10H | ; $B=16$ |
| :--- | :--- | :--- |
| Bigloop | PUSH BC | Save Value of $B^{-}$ |
|  | LD $B, 0$ | Set $B=256$ |

Naturally the DJNZ instruction does not have to be used: You could just as easily code this by setting " $\mathrm{BC}^{-}$to 1000 H , and used a short routine which decreased $B C$ and tested it for zero.

## Waiting Loops:

There are times in machine language programs when things happen so fast it is necessary to just wait a little while. Examples that spring to mind are sending information to a cassette (the pips have to be spaced sufficiently far apart to be able to read them later) or sending information to a typewriter (imagine printing thousands of characters a second!).

It is therefore useful to set up waiting loops using the DJNZ instructions:

Wait LD B, Count

The instruction "DJNZ Wait" will cause the CPU to jump back to the DJNZ instruction as many times as required to set "B' back to zero before proceeding again.

This should give you the answer to our exercise of what happens when you write:

Wait JR Wait
You might be waiting quite a while for the CPU to exit this loop!

INSTRUCTIONS FOR CALL
AND RETURN GROUP

| MNEMONIC | BYTES | $\begin{aligned} & \text { TIME } \\ & \text { TAKEN } \end{aligned}$ | C | 2 | EFFECT PV | $\begin{array}{r} \text { ON } \\ \mathrm{S} \end{array}$ | FLAGS | H |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CALL Address | 3 | 17 | - | - | - | - | - | - |
| CALL cc,Address | 3 | 10/17 | - | - | - | - | - | - |
| RET | 1 | 10 | - | - | - | - | - | - |
| RET cc | 1 | 5/11 | - | - | - | - | - | - |

Note: $c c$ is condition to be met for instruction to be executed. The following are the conditions which can be used:

| FLAG | ABBREVIATION | MEANING |
| :---: | :---: | :---: |
| CARRY | $\begin{aligned} & \text { C } \\ & \text { NC } \end{aligned}$ | Carry Set ( $=1$ ) <br> Carry Clear $(=0)$ |
| Zero | $\begin{aligned} & \mathrm{Z} \\ & \mathrm{NZ} \end{aligned}$ | $\begin{aligned} & \text { Zero Set }(=1) \\ & \text { Zero Clear }(=0) \end{aligned}$ |
| Parity | $\begin{aligned} & \text { PE } \\ & \text { PO } \end{aligned}$ | Parity even (=1) <br> Parity odd $(=0)$ |
| Sign | $\underset{P}{M}$ | $\begin{aligned} & \text { Sign Neg. }(=1) \\ & \text { Sign Pos. }(=0) \end{aligned}$ |

FLAGS EFFECTED:
Note that none of the flags are effected by the call or return instructions.

TIMING:
Where two times are shown, the shorter time indicated is for the case of the condition not being met.

The use of subroutines is as easy in machine language programming as it is in ordinary basic programs, if not easier.

In fact, remember that using the "USR" function in your basic program is really calling a subroutine: we need to have a "return" instruction to finish!

Therefore it is very easy for you to test certain subroutines independently of your main machine language program.

THE MAJOR DIFFERENCE THAT YOU WILL FACE IN IMPLEMENTING SUBROUTINES IN YOUR MACHINE LANGUAGE PROGRAM IS THAT IS IS NECESSARRY FOR YOU TO KNOW THE ADDRESS WHERE THE SUBROUTINE STARTS.

This can cause a problem if you store the machine language routines in a variable array, because the address of this variable is not necessarily fixed. See the last chapter on hints for storing programs which suggests that programs be stored in an array (so that they can be saved and reloaded) but moved to other addresses for execution.

Note that subroutines can also be called conditionally.
This is the machine language equivalent of the basic statement:
IF (condition) then GOSUB (address)

The difference is that the only conditions allowed are the status of four of the flags:

```
Carry flag
Zero flag
Parity flag (also overflow flag)
Sign flag
```

Remember that all these flags are set according to the last instruction which affected that particular flag.

It is therefore good practice to have "CALL" or "RETURN" instruction immediately after the instruction which sets the flag.
E.g.

| LD | $A$, (number) |
| :--- | :--- |
| CP | 1 |
| CALL | $Z$, one |
| CP | 2 |
| CALL | $Z$, two |
| CP | 3 |
| CALL | $Z$, three |

The above routine allows you to jump to various routines depending on the value stored in the location "number".

A shorter routine is possible if you know that there are only the above three possibilities for the value stored in number :

| LD | $A$, (number) |  |
| :--- | :--- | :--- |
| CP | 2 |  |
| CALL | Z,two | $; A=2$ |
| CALL | $C$, one | $; A<2 \Rightarrow A=1$ |
| CALL | three | $; A>2 \Rightarrow A=3$ |

This is because the instruction ${ }^{-C P} 2^{-}$sets both the zero and carry flags and the call instructions do not affect any flags.

Similarly the use of the conditional return from a subroutine is very useful.

## BLOCK OPERATIONS

You should by now be very familiar with the language your computer understands - it's very much like learning a foreign language: when you can think in that language you know you have mastered it.

This chapter covers the last set of very useful instructions - the next four chapters deal with instructions that are nice to have around and in some circumstances come into their own, but in general terms you should be able to write machine language programs with what you already know.

Be sure however to read the chapter on planning your machine language program!

The instructions covered in this chapter are by their very nature able to leap tall buildings in a single bound, faster than a speeding bullet - in other words, instructions which can operate on a block of memory rather than just single 8-bit bytes.

Let's start with the simplest of these:
CPI
With your knowledge of the 280 Language, you should be able to immediately recognise this is a member of the "compare" family, and it is in fact an extended compare.

It is read in english as "compare and increase"- (you will remember that one can only compare with anything with the contents of Register ${ }^{-} A^{-}$, and this does not need to mentioned in the instruction.)
"CPI" compares "A- with (HL) and increases HL automatically. This means that after the CPI operation, HL is already pointing to the next location ready for a repeat.

With such an instruction we might be able to

INSTRUCTIONS FOR BLOCK COMPARE AND MOVE GROUP

| MNEMONIC | BYTES | $\begin{aligned} & \text { TIME } \\ & \text { TAKEN } \end{aligned}$ | C | Z | $\begin{aligned} & \text { EFFECT } \\ & \text { PV } \end{aligned}$ | ON S | $\underset{N}{\text { FLAGS }}$ | H |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LDI | 2 | 16 | - | - | * | - | 0 | 0 |
| LDD | 2 | 16 | - | - | * | - | 0 | 0 |
| LDIR | 2 | 21/16 | - | - | 0 | - | 0 | 0 |
| LDDR | 2 | 21/16 | - | - | 0 | - | 0 | 0 |
| CPI | 2 | 16 | - | \# | * | * | 1 | \# |
| CPD | 2 | 16 | - | \# | \# | \# | 1 | \# |
| CPIR | 2 | 21/16 | - | \# | - | \# | 1 | \# |
| CPDR | 2 | 21/16 | - | \# | \# | \# | 1 | \# |

FLAGS NOTATION:
\# Indicates flag is altered by operation
0 Indicates flag is set to 0
1 Indicates flag is set to 1

- Indicates flag is unaffected


## TIMING:

For repeat instructions, the times shown are for each cycle. The shorter time indicated is for the case of the instruction terminating - eg. for CPIR, either $B C=0$ or $A=(H L)$.


Write a routine to search all of memory for a particular match, as follows:

Search CPI NZ, Search

In this way, unless a match is found (zero flag will be set as in all compare instructions) the program will keep on looking.

Unfortunately this is not such a good idea as unless a match is found the program would never end!

Fortunately the designers of the $Z 80$ language thought of this and the CPI instruction also automatically decreases BC!

We can therefore select at will the length of the block we wish to search through and thus specify an end to the search.

Let s assume that the length of the block we are searching through is less than 256 bytes long, so that the $B C$ count would only be stored in the $C$ register, we could write:

Search
CPI
JR Z, FOUND
INC C
DEC C
JR NZ, SEARCH
NOTFOUND
---
FOUND
Obviously a different routine would be implemented if the length of the block was more than 255 bytes. Note the use of the INC and DEC instructions to test whether $C=0$. These two instructions only require one byte each, and as they both affect the zero flag the net effect is to set the flag only if $C$ was originally zero. The other benefit is that coding does not alter any of the other registers.

Now we could also wish to search a block of memory starting from the top rather than from the bottom, and we therefore have the instruction:

CPD
Which is read in english as "compare and decrease". The decrease refers to HL of course, and the effect on $B C$ is still the same!

Even more powerful than these two instructions are the real supermen:
CPIR
CPDR
These are read as "Compare, Increase and Repeat"
and "Compare, Decrease and Repeat".
These 2-byte instructions are unbelievably powerful: they allow the CPU to automatially continue searching through the block of memory until either a match is found or the end of block is reached. (Naturally we have to specify $A, H L$ and $B C$ before starting, but even so this is unbelievably economical coding).

Because the instruction will stop for one of two possibilities (ie. match found in middle of block or no match found at all) we have to ensure we use some code at the end to differentiate between the two possibilities.

Users who are going to be writing machine code for the $2 \times 81$ and who wish to also make facility of the "SLOW" mode to enable continuous display should be very careful in using CPIR and other similar instructions as they can be very time consuming instructions.

CPIR, for example, requires 21 cycles for each byte to be searched. Admittedly there are $4,000,000$ cycles in each second, but even so this means that searching through 4,000 bytes requires $1 / 50$ th of a second.

This may not seem like a very long time to you but when you remember that the interrupt will also come every 1/50th of a second or so to display the screen the net effect is to cause a flicker in the screen. (This is because the interrupt cannot stop an instruction in the middle).

Experience has shown that instructions which take as little as 100 cycles (ie. searching through a block of 5 bytes!) can cause flickering, but of course only if the interrupt comes during execution of that instruction. You may have to weigh up the disadvantages of flicker against the possibility of that instruction being processed when the interrupt comes.

Typically the $2 \times 81$ in SLOW mode will process the program for about 1400 cycles before being interrupted. Thus an instruction with a time of a 100 cycles has a $7 \%$ chance of being executed when the interrupt comes.
*** *** $\star$ *

The remaining block operations are along the lines of "move it, mate".

These are:

| LDI | LDIR |
| :--- | :--- |
| LDD | LDDR |

Obviously part of the "Load" family these are read as:
LOAD AND INCREASE
LOAD, INCREASE AND REPEAT
LOAD AND DECREASE
LOAD, DECREASE, AND REPEAT
Taking the simplest one first, "LDI" is really a combination of the following set of actions:

LOAD (DE) WITH (HL)
INCREMENT DE, HL
DECREMENT BC
Note that this is the only instruction that will load from one memory location to another without having to be loaded into a register first.

The use of the "DE" register as the destination address is very clever this way you never forget which register holds the DE-STINATION!

The symmetrical instruction ${ }^{\text {}} \mathrm{LDD}^{\prime}$ is exactly the same except that $H \mathrm{~L}$ and DE are decreased as loading proceeds. The difference between "LDI" and "LDD ${ }^{-}$is more important when the two blocks ( the one where the information is and the one where the information is going) overlap.

Suppose we are using this instruction in a word processing application, and we want to delete a word from a sentence:

The big brown dog jumped over the fox.
If we now want to delete the word "brown" all we need to do is to move the rest of the sentence to the left by 6 characters.

$$
\begin{array}{ll}
\text { DE }=\text { DESTINATION } & =\text { CHARACTER } 9 \\
\text { HL } & =\text { SOURCE } \\
\text { BC } & =\text { COUNT }
\end{array}
$$

Let us start with LDI: after one instruction we have
The big drown dog jumped over the fox.
And
$H L=10, D E=16, B C=23$.
After 2 more instructions:
The big dogwn dog jumped over the fox.
And after all the instructions have been completed:
The big dog jumped over the fox.e fox.
(If we had wanted the portion after the full stop to be blanked out this could have been achieved by adding blanks at the end of the original sentence and increasing $B C$ to say 30.)

If we now want to reverse the process and return the word "brown" to the sentence, we cant simply use "LDI' again because we will overwrite the information we want to shift:
EG. HL = SOURCE = CHARACTER 9
DE $=$ DESTINATION $=$ CHARACTER 15
$B C=$ COUNT $\quad=24$ CHARACTERS.
After one instruction we would have:
The big dog judped over the fox.e fox.
After 6 instructions we would have:
The big dog judog juver the fox.e.fox.

So far so good. But another three gives:
The big dog judog jud og the fox.e.fox.
The problem is that we have overwritten the information we want to transfer.

We therefore have to use the "LDI' instruction, with the DE register pointing to the end of the sentence.

The instructions "LDIR" and 'LDDR' are even more powerful, able to shift thousands of bytes around very quickly.

## EXERCISE:

Write a short routine to transer 32 bytes from the ROM part of memory to the screen.
Be sure to define a line full of blanks in the basic program before calling the USR function.
ZX80 users could try moving 32 bytes from location OBCOH. ZX81 users could try moving 32 bytes from location 0190H.

ARE LESS FREQUENTLY USED
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## REGISTER EXCHANGES

We briefly discussed in the first few chapters the idea of the CPU having gloves it could put on or take off, and thus store some information in a place that is more accessible than memory locations.

You must remember that you cannot manipulate these alternate registers and the analogy with gloves is a very valuable one. While they will retain their shape, there is no way they can do any arithmetic or counting by themselves.

The first instruction is: EX AF, $\mathrm{AF}^{-}$


This does exactly what its name suggests: "Exchange the register pair AF and $\mathrm{AF}^{-1}$. In the gloves analogy we would say "Swap gloves on the pair of hands AF".

2X81 users should be extememly cautious about using this instruction. The manual states that the AF alternate register pair is used by the display routine and using the "EX AF, AF"" instruction may cause the program to crash. (This is because if the screen refresh comes when you have the wrong set of gloves on, the program will look for the information to be displayed in the wrong place).

The next general swap gloves instruction is:
EXX
This instruction swaps the gloves on all other 8-bit registers as follows:

| $B$ | $C$ |  | $B^{-}$ | $C^{-}$ |
| :--- | :--- | :--- | :--- | :--- |
| $D$ | $E$ |  | $D^{-}$ | $E^{-}$ |
| $H$ | $L$ |  | $H^{-}$ | $\mathbf{E}^{-}$ |

This is therefore a very powerful instruction but its very power makes it limited in use. This is because it acts on all the registers at once and it is not possible to hold any value back. (Except in register " $A$ " which is not affected by "EXX").

The only way around this problem is to write a short routine along the lines of:

| PUSH | HL |
| :--- | :--- |
| EXX |  |
| POP | HL |

This means that you have saved the values of $B C, D E$ and $H L$ in the alternate set of registers but still have HL's value to work with.

The last instruction in this group does not really fall within the swap gloves type:

EX DE, HL
In this instruction DE gets the contents of HL and HL the contents of DE .

This instruction is indeed very useful, because as we saw HL is a favoured register pair in many applications and there are times when the value we want to manipulate is in $D E$.

## BIT, SET AND RESET

So far all the instructions we have been dealing with have involved the manipulation of 8 -bit or 16 -bit numbers.

The "Bit, Set and Reset" group allows us to manipulate the single bits of registers of contents of memory locations. Because of the very tedious nature of fiddling with single bits this is not a very commonly used group of instructions.

Furthermore, it tends to take even longer to set a single bit in a register or memory location than it does to change or examine the entire 8 bits of that memory location or register.

Nonetheless there are times when you need to know whether a bit in the middle is set or not, or even to set a bit. Note however that many of the bit setting or resetting can be carried out using the logical operators.

The "Bit, Set and Reset" group of instructions allows us to turn any bit "on" or "off" at will, or even just look at a specified bit to see what its status is.

Let us look at the first set of instructions:

| SET | $n, r$ |  |
| :--- | :--- | :--- |
| SET | $n$, | $(H L)$ |
| SET | $n$, | $(I X+d)$ |
| SET | $n$, | $(I Y+d)$ |

The "SET" instruction turns "On" (i.e. = 1) the bit numbered " $n$ " (using the notation $0-7$ ) in register " $r$ ' or in the specified memory location.

No changes are made to any of the flags.
The "RESET" group of instructions operate on exactly the same range of registers or memory locations, but instead of turning the bits " 0 n ", it turns the bits "Off" (i.e. = 0).

The "BIT" instructions should really be read as "BIT?" in English as the function of this instruction is to test the contents of the indicated bit.

No changes are made to the registers or memory locations but the zero flag is altered according to the status of the bit tested.

$$
\left.\begin{array}{lll}
\text { If Bi.t }=0 & \text { then } & \text { zero flag is set on }(=1 \\
\text { If Bit }=1 & \text { then } & \text { zero flag is set of } f(=0
\end{array}\right)
$$

This may seem confusing at first glance but think of it this way: if the bit is zero, then the zero flag is raised; if the bit is on, then naturally the zero flag would not be raised.


## ROTATE AND SHIFTS

You can move them to the left, you can move them to the right, you can shift those registers any which way you like.

The trick is to differentiate between the various shifts and rotate in order to know which one to use when and to remember that the "Carry" bit can often be considered to be a 9th bit of the registers. (I.e. the Carry is bit 8 if the bits are numbered $0-7$ ).

Some rotate instructions go right through the Carry (as the 9th bit) so that the entire rotation goes through a cycle of 9 bits. For example, let us look at "RLA" (the meaning of each instruction will be made clear later in this chapter):


Other rotations involve only an 8-bit cycle, although the carry flag is changed according to the bit which has to go the "Long way round". An example of this is the "RLCA" instruction:


This means that in a left rotation as above the contents of bit 0 are transferred to bit 1, bit 1 to 2, etc., but the contents of bit 7 are transferred to both the carry bit and to bit 0 . Compare this with the "RLA- instruction above where bit 7 gets transferred to the carry bit and the carry bit gets transferred to bit 0 .

## LEFT ROTATIONS:

There are basically two types of left rotations:

* ROTATE LEFT REGISTERS - this is a 9-bit cycle rotation as illustrated above for "RLA"

> RLA - "Rotate left accumulator"

RL r - "Rotate left register $\mathbf{r "}^{\prime \prime}$


* ROTATE LEFT CIRCULAR - the "Circular" means that the cycle is only 8bits as with the RLCA instruction illustrated above.



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As well as these two left rotate instructions there is a SHIFT LEFT instruction available, but this can only operate on register ${ }^{-} A^{-}$:

SLA - shift left accumulator


This is different in that the contents of the carry bit are lost and bit zero is filled with 0 . This is effectively multiplying " $A^{-}$by 2 as long as nothing is transferred to the accumulator. (Think about ${ }^{\circ} \mathrm{SLA}^{-}$if $A=80 \mathrm{H}$ ).

## RIGHT ROTATIONS:

Once again we have the two basic modes of rotations but this time to the right. Exactly the same range of possible memory locations and rotations can be spinned to the right as to the left.


A similar shift right is available as for shift left:
SRL $r$ - Shift right logical register " ${ }^{\prime}$ "


In this case this is pure division by 2 as long as we are using unsigned numbers (i.e the number range we wish to represent is $0-255$ ).

Because in some applications we use the convention to indicate negative numbers by setting bit 7 to 1 (i.e giving us a range of -128 to +127 ) there is an addition shift right instruction called SRA r - Shift right arithmetic "r"


As you can see this is also division by 2 but it preserves the sign bit.

In and Out is just about as simple a concept as you could get in machine language programming.

There are times when the CPU needs to get information from the outside world ("No CPU is an island?"), such as from the keyboard or from the cassette player.

As far as the CPU is concerned that's totally foreign territory and as all good CPUs it will never leave home. The most it is prepared to do is to open a door to allow deliveries. The CPU doesn ${ }^{-t}$ know and doesn ${ }^{-t}$ care to know how a cassette player works.

All the relevent information is which door the cassette man is going to be delivering his goodies to - there is a choice of up to 256 doors for the 280 chip but the actual number available to a particular CPU is a result of decisions made by the hardware manufacturers. As far as the Sinclair is concerned there is only the keyboard, the printer and the cassette player.

The other thing the CPU doesn ${ }^{-1}$ t want to know about is how the data is being transmitted. As far as it's concerned, if it's coming in or going out, it's an 8-bit byte.

The keyboard is on the other side of door FE , so that to get data in from the keyboard you use the instruction

$$
\text { IN } A,(F E)
$$

Now you may be asking yourselves how the 40 keys of the keyboard are arranged so as to be represented by 8-bit bytes.

The answer is not what you would expect - the keyboard only returns information from 5 keys at a time. It is the value of " $A$ " as the door is opened which determines which set of 5 keys are going to be examined!

The keyboard is divided into 4 rows, each comprising two blocks of 5 keys:


You can see that there are 8 blocks of letters and we should therefore be able to correlate this with the 8 bits of " $A$ ". This is in fact the case:

All of the bits of " $A$ " are set to ${ }^{\text {" } O N \text { " except for one bit which specifies }}$ the block to be read.

You can think of it as something like a secret handshake - as the CPU goes to the door to get the information the handshake determines which piece of information it gets.

Thus to read the keys in the block " 12345 ", it is bit 3 of " $A^{\circ}$ which should be off:

$$
A=111100111=F 7
$$

The contents of the keyboard are returned in " $A$ " with the information coming into the lower bits of " $A$ ":
i.e Key ${ }^{-1}{ }^{-1} \rightarrow$ bit 0 of ${ }^{-} A^{-}$

Key ${ }^{-2}{ }^{-} \rightarrow$ bit 1 of " $A$ "
If block 4 was chosen instead (i.e $A=E F$ ) then the information would come in as:
$\begin{array}{lllll}\text { Key }{ }^{-} 0^{-} & \text {bit } 0 \text { of } A^{-} \\ \text {Key } & 9^{-} & \text {b }\end{array}$
Key ${ }^{-9} 9^{\prime} \rightarrow$ bit 1 of ${ }^{\prime} A^{\prime}$
You can think of the information coming into " $A$ " from the outside edges first, so that both ${ }^{-} O^{-}$and " $1^{\text {- }}$ would both go to bit " $O^{-}$of register " $A^{\prime}$.

For some games applications you may wish to allow all of the top row to be read, and it it possible to read it all in one instruction (rather than the two instructions which would be required if we read one block at a time).

This is done by fooling the doorman into giving you two lots of information at once:
e.g. $\quad A=11100111=E 7$

Note that both bits ${ }^{-} 3^{\prime}$ and ${ }^{-1} 4^{\circ}$ are ${ }^{\circ}$ of $f^{\circ}$.
This handshake tells the doorman that the CPU wants the information from block 3 and block 4, and that is what it will get. Of course the two lots of information get jumbled and it is not possible for you to tell whether

i.e. $\quad-1^{-}$or $0^{-} \rightarrow$ bit 0 of $A$
${ }^{-} 2^{-}$or ${ }^{-9} 9^{-} \rightarrow$ bit 1 of $A$
etc
This is useful in movement games because it enables keys ${ }^{-5} 5^{\prime}$ and ${ }^{-8 \prime}$ to be used as the left and right direction arrows even though they belong to different blocks in the keyboard.

Note that if you use the instruction

$$
\text { IN } R, \text { (C) }
$$

where register " $C$ - specifies which door you want, then it is the contents of register " $B$ " which define which keyboard block is being selected.

The other doors which will be of interest to those people trying to write a routine to enable them to load data or save data on cassette (it can be done) are obviously the cassette input/output doors.

These are doors " $\mathrm{FF}^{\prime}$ for sending information to the cassette, and door -FE' for getting information in, but the major problem involved is the timing of the data going out and going in. This kind of problem requires a lot of experience with machine language programming and calculations of the time required for each instruction path.

PROGRAMMING

## YOUR SINCLAIR



## PLANNING YOUR MACHINE LANGUAGE PROGRAM

Machine language programming is extremely flexible in that it allows you to do anything at all.

Since all the higher level languages ultimately have to come down to machine language, it follows that anything you can program in Fortran or Cobol or any other language can be done in machine language.

With the additional benefit that the machine language program will be the faster one.

This total flexibility can however also be a trap to the unwary programmer. With so much freedom, it it possible to do anything. Unlike the Sinclair's basic operating system, for example, there are no checks on whether the statement is a legal one.

Since all numbers you can enter will be an instruction of one kind or another, the $\mathbf{Z 8 0}$ chip will process everything.

But even beyond the problems of checking whether the Syntax is legal, machine language programming has no constrains on your logic - you can perform functions, jumps, etc which would be totally illegal in any higher level language.

It is therefore of the utmost importance to discipline yourself in the design of machine language programming. I cannot recommend too highly the concept of the "top-down" approach in programming in general, but especially in machine language programming.

The "Top-down" approach forces you to break down the problem into smaller units, and enables you to check the logic of your design without doing any coding for a long time.

Suppose you wanted to write a lunar lander program:
The very first approach might be something along the lines

| Instr | Display instruction Jump back to instr till n/line pressed |
| :---: | :---: |
| Draw | Draw landscape, start lander at top |
| Land | Move lander |
|  | If fuel finished go to crash |
| Ground | Print congratulations |
|  | Jump back to instr for next go |
| Crash | Print commiserations on bad landing |
|  | Jump back to instr for next go |

Notice how this "program is written totally in English. At this stage, no decision has been made whether the program is to be written in BASIC or machine language. Nor is it necessary to make that decision - the concept of the lunar lander program is not dependent on the coding.

Now comes the part of logic testing.
You play the part of the computer and see if all the possibilities you wish to see included in the program are covered.

Are there any jumps to things you meant to write in but forgot? Is everything there? Are some routines redundent? Should some of the things be put into subroutines.

Let us look at the "program" again - oh, oh: we forgot to allow any way to finish the program!

The above logic might be fine for some applications, such as an arcade machine, but in your program you decide you would like to be able to turn the program of $f$.

We now change the last part of the program as follows:

| Ground | Print congratulations |
| :--- | :--- |
|  | Jump to finish |
| Crash | Print commiserations on bad landing |
| Finish | Ask player if finished |

If no, Jump to instr
If yes, stop
Note that we have used labels to describe certain lines in the program. These are very valuable, the more so if you choose short labels which are descriptive in their meaning.

Once this level is finished, you move one level down to do the same thing to one of the lines or modules above.
This is why this approach is called the Top Down approach.
For example, we can expand the "finish" module above:

| Finish | Clear screen |
| :--- | :--- |
|  | Print "Would you like to stop now?" |
|  | Scan keyboard for input |
|  | If input $=$ yes then stop |
|  | Jump to instr |

The other benefit of the top down approach is that you can test and run a particular module on its own, so that is is ready for the final program.

Let us go down one level further again, and look at the
Clear screen
line in more detail.
By this stage we do have to decide on what language we will write the program in, and let us choose machine language on the Sinclair.

If you were writing in BASIC, all you would have to say is : 900 CLS, but in machine language that simple sentence, "Clear Screen ${ }^{-}$can be deceptive (because of the way the Sinclair uses the screen display we must remember to fill in the end of lines!).

We might therefore do something like:
Clear Find screen beginning
Fill next 768 positions with blanks
Get screen beginning again

```
Fill that byte with "End-Line`
For lines 1 to 24
| Skip next 32 bytes
! Fill next byte with `End-Line`
Next line
```

We still haven ${ }^{-t}$ done any coding, but obviously the approach is based on machine language. The next level down is the one which does the coding, so let us look at filling the screen with blanks:

Clear LD HL, (Screen) ;Screen start
LD BC, 768 ;Bytes to clear

LD D,0 ;D = blank
Loop LD (HL),D ;Fill blank
INC HL ;Next position
DEC BC ;Reduce count

LD A,B
OR C ; Test if $\mathrm{BC}=0$
$J R \mathrm{NZ,Loop} \quad ;$ Again if not end
Now you can deal with programs of such length quite easily and in this way build up very complex programs indeed.
By the way, you no doubt understand now why machine language programs tend to be so long and why people invented the higher language programs!

## EXERCISES:

There are more ways than one to write any particular routines, so let us look at the simple clear screen routine written above.

This could be handled by several different approaches.

## EXERCISE 1:

Can you think of a way that would enable the Loop to blank 768 positions without using the $B C$ register, but using the $B$ register only so that we may make use of the " $D J N Z$ ' instruction?

## EXERCISE 2:

Can you think of a way that would enable the 768 positions to be blanked using the more powerful "LDIR" instruction?

Think carefully of what "LDIR" does: It is not always necessary to have 768 blank positions elsewhere!

ANSWERS:
More than one possible answer can be "right" - the only test is does it work?

USING DJNZ:
CLEAR
LD HL, (SCREEN)
LD A,0
LD B,A ;SET B=256
LD (HL),A ;
INC HL ;FILL IN
LD (HL),A ; $3 \times 256$
INC HL ; BYTES
LD (HL),A
INC HL
DJNZ LOOP
USING LDIR:
CLEAR
LD HL,(SCREEN) ;SOURCE
PUSH HL
POP DE
INC DE $\quad$;DEST $=\mathrm{HL}+1$
LD BC,768 ;HOW MANY
LD(HL), $0 \quad$;1ST POS $=0$
LDIR ;MOVE IT
If you add up the memory required, the first two methods each require 14 bytes and the last 13 bytes.

## DEBUGGING AND EDITING

## YOUR MACHINE LANGUAGE PROGRAM

The first issue for you to consider after you have designed your program and know what it is you want it to achieve is for you to decide where to put it in memory.

Sounds simple? Not really on the Sinclair $Z X 80$ or $Z X 81$. If your program is only a few lines long, then there may not be any problem. You can just enter it again using "Poke" commands, either manually or through a BASIC program just for that purpose.

In this case, all you need is to have spare "RAM" memory for your program:
1000 LET PROGRAMSTART $=17000$
1010 FOR I = 0 TO PROGRAMLENGTH
1020 POKE PROGRAMSTART+I, DATA(I)
1030 NEXT I
The machine code values are stored in an array specially set aside for this purpose. Note that this is fine for a short program, but not very efficient because each machine code byte occupies one variable location: This is 2 bytes on the $Z \times 80$ and 5 bytes on the $2 \times 81$.

The following are the possible storage locations for machine language programs:

FREE RAM MEMORY
REM STATEMENT
PRINT STATEMENT
VARIABLE ARRAYS
Each of these has certain advantages and disadvantages, so let us examine each in turn.

## A. FREE RAM MEMORY

This is OK for very short programs but the disadvantages are:
RAM MEMORY IS SET TO ZERO

CANNOT BE SAVED ON TAPE>
These disadvantages make it almost impossible for programs of any length to be debugged or run from free' RAM:

## B. DIRECT CODE - POKED` INTO REM STATEMENT

Using this method, the actual code values are poked directly int the REM statement.
A line in the Basic program (usually the first one, so that its location in memory is known) is set up at the beginning with as many characters as expected in the machine language program.
EG. 100 REM AAAAAA $---\left(128 A^{-} S\right)$
----AAAAAA
110 ETC.
The actual contents of the REM statement is not important - you can use A, $X$, graphic characters or whatever.

ADVANTAGES:
STARTING ADDRESS IS KNOWN
(THIS IS VERY VALUABLE FOR SUBROUTINES)
CODE IS IN DIRECT FORM FOR RUNNING.
DISADVANTAGES:
DIFFICULT TO INSERT ADDITIONAL CODE.
SOME CHARACTERS ARE UNLISTABLE (OLD ROM ONLY - CAUSES PROBLEMS.)
PROGRAM HANGS UP IF ${ }^{-118}{ }^{-}$IS POKED IN EG> CP 118.

Nonetheless this method offers many advantages, and is especially useful for storing subroutines which have already been debugged.

## C. HEX CODE STORED IN REM STATEMENT OR IN PRINT STATEMENTS:

In this situation, the direct code is not stored but rather the hexidecimal representation.
EG.

OR 560 PRINT "CDAO1 -- ETC --"
This means that you need to have part of your Basic program (or a special USR routine) devoted to translating the hexidecimal representation and then poking the codes into free memory or into arrays as required.

As many lines a necessary can be used. You might decide to have 16 instructions/basic line, or have each line contain a particular subroutine or module for easy manipulation.

ADVANTAGES:
-LISting ${ }^{\text {C }}$ CAN BE EASILY VIEWED
INSERTIONS AND DELETIONS ARE EASY
DISADVANTAGES:
PROGRAM CODE TAKES THREE TIMES AS MUCH ROOM AS CODE ONLY WOULD

SPECIAL LOADING ROUTINE REQUIRED.
USE OF LOADING ROUTINE REQUIRED WITH everr alteration to code.

Despite its advantages this is probably the best way to develop and debug long programs. Once they have been fully tested, the REM or PRINT statement is no longer required and the code can be stored as direct code in a REM statement or in an array.

## D. DIRECT CODE STORED IN AN ARRAY

This is probably the best place to store your machine code program once it has been fully debugged and tested - except for subroutines!

An array is dimensioned as the first line of the "Basic" program: 100 DIM A(100)
In this way, the array is the first variable to be stored and its starting can be obtained by using the system variables.

The code is "Poked" into the array either by the "Basic" program or by you.

The main benefit stems from the fact that the code can then be easily "saved on to tape and is ready to run. You also have the protection of other people not being to read your code easily.

ADVANTAGES:
VERY COMPACT MODE OF STORING
NO BASIC PROGRAMMING NEEDED
PROGRAMS CAN BE SAVED
NO PROBLEMS WITH SCREEN display

## DISADVANTAGES:

STARTING ADDRESS MUST BE COMPUTED
(MAKES SUBROUTINES IMPOSSIBLE)
DIFFICULT TO EDIT
limited in lengit to max array
MAJOR POINTS TO WATCH OUT FOR:
One of the worst pitfalls in testing and debugging machine language programs comes from the relative jump instructions.

Although these instructions are very powerful and extremely useful, they do make life somewhat difficult whenever a change has to be made.

At all times check that your calculations of the relative jumps are correct before running a program - one wrong calculation and your computer will display the "Lost in Space" syndrome.

This means that when you are debugging a program, you must be especially careful not to insert or delete any instructions without first checking that these changes will not effect any relative jumps!

As it's almost impossible to keep all these things in mind as you try to work out why the perfect program isn ${ }^{-t}$ functioning, it is a good idea to follow the following rules:

```
WHEN DELETING INSTRUCTIONS, REPLACE
    THE UNWANTED CODE BY \({ }^{-}\)NOP \({ }^{-}(=00)\).
    IF INSERTING CODE LONGER THAN ORIGINAL
    USE 'JP PATCH" ( = C3 DD DD).
```

The "NOP" is a very valuable instruction that we did not deal with in any of the earlier chapters.

The "NOP" instruction means "NO OPERATION", and you can have as many of these as you like anywhere in your program without damage.

The code for "NO OPERATION" is so simple, you"ll never forget it - ZERO!
When your program is finished and working to your satisfaction, you can clean things up by deleting all these "NOP' -after working out the new relative jumps of course.

Inserting new code is more difficult, and involves patching. It cannot be recommended too highly for you to keep a notebook of editing you are making as you go along, so that when your program is working, you can bring back a semblance of order!

The "JP PATCH" instruction is three bytes long, so make sure any code you are replacing is included in the patch.
E.G. Original Code =

17300 LD B,56
LD HL, 17312
But you decide that you really need to load BC not only B at location 17300.

The original instruction is 2 bytes, while
LD BC, 56
is a three byte instruction.

Let us look at the actual memory location contents:
$17300 \quad 06$
$17301 \quad 38$
1730201
17303 AO
$17304 \quad 43$;LD HL,17312
The solution is to put in the -JP PATCH INSTRUCTION` at 17302. because this then destroys the first byte of the "LD HL, 17312" instruction, we must now delete that instruction and include it in the patch.

The new listing will look like:
17300 JP 19000 ;JUMP TO PATCH

19000 LD BC,56 ;CORRECT CODE
LD HL, 17312
JP 17303 ;RETURN TO MAIN
Let us look at the memory locations again:
17300 C3
1730138
17302 4A
$\begin{array}{lll}17303 & 00 & \text {;NOP } \\ 17304 & 00 & \end{array}$
1900001
1900100
1900238
etc.


## DISPLAYING 100 BYTES IN HEX

ZX 81 VERSION
100 PRINT "ENTER START"
110 INPUT S
120 LET $S=$ INT $(S / 10)$
130 CLS
140 FOR R $=\mathbf{S}$ TO $S+9$
150 PRINT "="; 10*R ; ">"
160 FOR I = 0 TO 9
170 LET $V=\operatorname{PEEK}(10 * R+I)$
180 LET $H=$ INT (V/16)
190 LET L $=V-16^{*} \mathrm{H}$
200 PRINT CHR\$(H+28); CHR\$(L+28); " ";
210 NEXT I
220 PRINT
230 NEXT R
240 PRINT
250 PRINT "NEXT 100?"
260 INPUT I\$
270 LET $S=S+10$
280 IF CODE (I\$) $=62$ THEN GO TO 130

2X 80 VERSION
Enter program as above, but alter lines 120 and 180 to read as follows:
120 LET $S=S / 10$
180 LET $H=V / 16$

## MACHINE CODE EDITOR

## ZX81 VERSION

```
100 PRINT "START?"
110 INPUT S
120 CLS
130 PRINT "MEMORY";TAB 10;"CODE"
140 FOR I = O TO 10
150 LET V = PEEK (S+I)
160 GO SUB 500
170 PRINT S+I; TAB 7; A$;
180 INPUT A$
190 IF A$ = "" THEN GO TO 220
200 LET V = 16 * CODE (A$) + CODE (A$(2)) - 476
210 POKE S+I, V
220 LET V = PEEK (S+I)
2 3 0 ~ G O ~ S U B ~ 5 0 0 ~
240 PRINT TAB 10; A$
250 IF V = 201 THEN GO TO 270
260 NEXT I
270 PRINT "CHANGES?";
280 INPUT A$
290 IF CODE (A$) = 62 THEN GO TO 120
300 PRINT " MORE?"
310 INPUT A$
320 LET S = S + 10
330 IF CODE (A$) = 62 THEN GO TO 120
340 CLS
350 PRINT "START FOR USR?"
360 INPUT S
370 PRINT USR (S)
380 STOP
500 LET H = INT (V/16)
510 LET L = V - 16 * H
520 LET AS = CHR$ (H+28) + CHR$ (L+28)
530 RETURN
```

NOTE: This program will fit into the standard 1 K ZX81 machine and allow code to be entered in hexadecimal format into free memory, "REM statements (e.g. Line 90 REM AAAAAAAAAAA ), or into variables (e.g. Line $90 \operatorname{DIM} A(4)$ ).

This program will also "RUN" the machine language program if required. If you do not desire to "RUN" the program, reply "XX" to query "START FOR USR?"

## MACHINE CODE EDITOR

ZX 80 VERSION

```
100 PRINT "START?"
110 INPUT S
120 CLS
130 PRINT "MEMORY","CODE"
140 FOR I = O TO 20
150 LET V = PEEK (S+I)
160 GO SUB 500
170 PRINT S+I, CHR$(H);CHR$(L);" ";
180 INPUT A$
190 IF A$ = "" THEN GO TO 220
200 LET V = 16*CODE (A$) + CODE (TL$(A$) ) - 476
210 POKE S+I, V
220 LET V = PEEK (S+I)
230 GO SUB 500
240 PRINT CHR$(H);CHR$(L)
250 IF V = 201 THEN GO TO 270
260 NEXT I
270 PRINT "CHANGES?",
280 INPUT A$
290 IF CODE (A$) = 62 THEN GO TO 120
300 PRINT "MORE?"
310 INPUT A$
320 LET S = S+20
330 IF CODE (A$) = 62 THEN GO TO 120
340 CLS
350 PRINT "START FOR USR?"
360 INPUT S
370 PRINT USR (S)
380 STOP
500 LET H = V/16
510 LET L = V - 16*H + 28
520 LET H=H + 28
530 RETURN
Note: This program will fit into the standard 1 K ZX80 Machine and allow code to be entered in hexadecimal format into free memory, "REM" statements (eg. line 90 REM AAAAAAAAAAA ), or into variables (eg. line 90 DIM A(10) ).
This program will also "RUN" the machine language program if required. If you do not desire to "RUN" the program, reply "XX" to query "Start for USR?"
```


## FROM REM LINE TO ARRAY

The following program is for the $2 \times 81$ with additional memory. (A modified version of this program can easily be written for the $2 \times 80$.) Use the "Machine Code Editor" program and add the following lines:

```
90 REM AAA -- at least 52 chars --- AAA
100 DIM A(100)
```

Add the following lines at the end of the program as dummy code:
1000 REM ABCD
1010 REM 1234
The aim of this program is to transfer the code in the REM lines starting at line 1000 into the Array " $A^{\text {" }}$. The REM lines can be any length; the only requirement is that code is entered in hexadecimal format - the program will crash if you do not have code as 2-digit pairs.

Now <RUN> the program and answer 16514 to the query "START?". 16514 is the location of the first usable character in the REM statement in line 90.

Enter code as overleaf, and when finished answer 16514 to query "Start for USR?". The 4 dummy codes should be transferred to the Array. To check on this, enter the following line without line number:

PRINT PEEK $16400+256$ * PEEK 16401 <NEW LINE>
This will return the address of the start of Array "A". Enter <GOTO 100> <NEW LINE> and answer that address for "START"?.

Note: Do not use <RUN> or <GOTO 1> as this will redimension Array "A" and set all values to 0 .

Contents of memory should be:


MACHINE CODE:

| DD 2A 104 |  | LD IX, (16400) | START OF ARRAY |
| :---: | :---: | :---: | :---: |
| 010041 |  | LD BC, 16640 | POINTER BEFORE <br> LINE 1000 |
| 03 | FREM | INC BC |  |
| OA |  | LD A, (BC) |  |
| FE EA |  | CP EAH | IS THIS REM? |
| 20 FA |  | JR NZ, FREM | IF NOT, AGAIN |
| 03 | NXTLIN | INC BC |  |
| OA |  | LD A, (BC) | TAKE 1ST CHAR |
| D6 1C | NXTCHR | SUB 28 | SUBTRACT 28 |
| 07 |  | RCLA |  |
| 07 |  | RCLA |  |
| 07 |  | RCLA |  |
| 07 |  | RCLA | MULTIPLY BY 16 |
| 6F |  | LD L,A | TEMP STORE |
| 03 |  | INC B |  |
| OA |  | LD A, (BC) | NEXT CHAR |
| 061 C |  | SUB 28 | SUBTRACT 28 |
| 85 |  | ADD A,L | ADD VALUE OF 16*1ST CHAR |
| D0 7106 |  | LD (IX+6), A | STORE IN ARRAY |
| 0023 |  | INC IX |  |
| 03 |  | INC BC |  |
| 0A |  | LD A, (BC) | TEST IF END |
| 2E 75 |  | LD L, 75 H |  |
| 2 C |  | INC 1 | $L=76 \mathrm{H}$ |
| BD |  | CP L | END OF LINE? |
| 20 E1 |  | JR NZ,NXICHR | IF NOT, GET NEXT CHAR |
| 03 |  | INC BC |  |
| 03 |  | INC BC |  |
| 03 |  | INC BC |  |
| 03 |  | INC BC |  |
| 03 |  | INC BC | SKIP LINE NO. |
| OA |  | LD A, (BC) |  |
| FE EA |  | CP EAH | IS IT REM? |
| CO |  | RET NZ | FINISH IF NOT |
| 18 DA |  | JR NXTLIN | ELSE GET CHARS |
|  |  |  | from next line |

It is possible for the standard 1 lK Sinclair $\mathbf{Z X 8 1}$ to play draughts! Of course, this is only possible by using every trick in the book. (A similar machine language program could be written for the $\mathbf{Z X 8 0}$ ).

The board is shown on the screen as follows:

| 1 | 1 | B |  | B |  | B |  | B |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2 | B |  | B |  | B |  | B |  |
| 3 | 3 | B |  | B |  | B |  | B |
| 4 |  |  |  |  |  |  |  |  |
| 5 | 5 |  |  |  |  |  |  |  |
| 6 | W |  | W |  | W |  | W |  |
| 7 | 7 | W |  | W |  | W |  | W |
| 8 | W |  | W |  | W |  | W |  |
|  | A | B | C | D | E | F | G | H |

(The outer numbers 1-8 and the designation of columns A-H are not shown on the screen - the only numbering included are the numbers $1,3,5$ and 7 as shown within the board).

The rules of the game the $\mathrm{Zx81}$ plays follows the standard rules except that multiple jumps are not allowed and capture is not compulsory.

Reaching the end line results in the creation of a king (shown on the screen as inverse letter), which can only move one square at a time but is allowed to jump backwards.

## STRUCTURE OF THE PROGRAM:

In the standard 1 K version there is also insufficient room to retain the string variable that initially sets up the board in the program listing. We must therefore resort to putting that string variable in memory and using <GOTO l> to start the program.

The last space saving "trick" involves replacing all 1- and 2-digit numbers in the listing: each number in a $\mathrm{ZX81}$ listing takes up 6bytes! This is true even if your number is only a single digit. We therefore make liberal use of constructs such as VAL"2" or CODE"W" which only require 4 bytes.

The program is also broken down into 3 different programs, the last two of which overlay the previous ones. This is the only way to enter so much information into the Sinclair $2 \times 81$ 1K.

The structure is as follows:
Program 1: PUT MACHINE CODE ROUTINE INTO REM STATEMENT

Program 2: DEFINE THE BOARD FOR PLAY
Program 3: DRAW THE BOARD
INPUT PLAYERTS MOVE CHECK PLAYER MOVE VALIDITY
MAKE COMPUTERS MOVE
(CALL TO USR ROUTINE)
GO TO NEXT PLAYER INPUT

## DRAUGHTS:

PROGRAM 1:
100 REM 11111111111111111111111
111111111222222222222222222222222
222222222333333333333333333333333
333333333444444444444444444444444

The REM statement
must have 175 chars
in it.

444444444555555555555555555555555 55555555566666666666666666

This part of the program is to input the machine language code into the REM statement. The code is listed at the end of this section, commencing at location $4082 \mathrm{H}=16514$. Use a modified version of the machine code editor to enter this code into the REM statement.

Once you have entered the machine language code, the listing of the machine code editing program is no longer required.

## DRAUGHTS

## PROGRAM 2

At this stage you should have only line 100 from the program above contianing the machine code. Add the following lines:


The graphics character is obtained
by using GRAPHICS and <Shift> <A>
150 FOR L = VAL "1" TO VAL "8"
160 PRINT AS ( TO VAL "8" )
170 LET AS = AS (VAL "9" TO )
180 NEXT L
200 INPUT AS
310 IF USR 16514 > VAL "0" THEN GOTO 200
This program will display the board on to the screen and test the machine language routine entered in Program 1.

The screen is saved in the string variable A\$, and is printed in 8 lines. It is essential that a minimum configuration screen is set up, so that the structure in memory of the board is as follows:

(where the symbol $B_{\text {is }}$ is used to represent END-OF-LINE). If you check this out this means that all legal moves are limited to increases and decreases of 8 or 10 bytes in memory.

Users with additional memory connected to the $\mathbf{Z X 8 1}$ should add the following lines:

130 POKE 16389, 76
140 CLS
This will ensure that a minimum configuration screen is set up.

## RUNNING PROGRAM 2

Press <RUN>. The screen will be displayed as shown above, and the $2 \times 81$ will be waiting for a string input. Press <NEW LINE> to see the computer's first move. You should see the computer move its first piece from G3 to H4.

You can continue to press <NEW LINE> to see what the computer would do next if that was its position. If you so desire you can change the string variable in 120 to set up any starting position.

PREPARING FOR PROGRAM 3
Enter the following line into your listing:
130 STOP
and then press <RUN>. Delete lines 120 and 130 and SAVE your program so far.

This has the effect of storing the string variable in memory without the need to keep it in the program listing. (Users with more than 1 K memory do not need to do this - retain your original lines 120 - 140).

DRAUGHTS
program 3
At this stage you should have lines 100, lines 150-180, and lines 200 and 310. The string variable $\mathrm{A} \$$ is stored in memory, so do not press <RUN> or <CLEAR> as this will destroy the contents of A\$.

Add the following lines to your program:

```
210 LET S = PEEK 16396 + VAL "256" * PEEK 16397
220 LET F = S + CODE AS + VAL "9" * CODE A$
    (VAL "2" ) - VAL "298"
230 LET T = S + CODE AS (VAL "3" ) + VAL "9" *
    CODE A$ (VAL "4" ) - VAL "298"
240 LET M = (T + F) / VAL "2"
250 IF (PEEK F <> CODE "W" AND PEEK F <> CODE
    "W") OR (ABS (F-T) > VAL "10" AND PEEK M <>
```

```
    CODE "B" AND PEEK M <> CODE "B" > OR (PEEK F
    < CODE "X" AND F<T ) OR PEEK T <> CODE "m" THEN
    GOTO 200
    Letters in squares are inverse
    characters obtained using GRAPHICS
    mode.
270 POKE T, CODE "W" + CODE "■" * (PEEK F )
    CODE "W" OR (T-S) < VAL "9")
    The graphic character in this line
    is obtained in GRAPHICS mode by
    pressing <Space>
    POKE F, CODE "⿴囗十介
    IF ABS (F-T) > VAL "10" THEN POKE M, CODE "R⿱⿱⿴囗冂一贝:8"
    PAUSE CODE "W"
```

PLAYING DRAUGHTS：
As we mentioned at the beginning，if you only have 1 K you cannot use＜RUN＞ as this will clear the variable so carefully saved．Use＜GOTO l＞instead． （Users with additional memory have the string variable in the listing so can use＜RUN＞．）

You should already have tested Program 2 by the time you come to this point，so you already know the display routine works and the machine language routine works．The additions in Program 3 are the player＇s moves and checking if these moves are allowed（This is all in line 250：＂F＂is ＂from＂and＂T＂is＂to＂）．

The input the computer is waiting for is a 4 －character string，such as ＂A6B5＂．This means that you mean to move from square A6 to square B5．

As only the most rudimentary numbering has been included in the screen， you may find it useful to keep a properly numbered board by the computer when playing．

If you should wish to play a second game，you cannot simply use＜GOTO 1＞ again，as the string variable AS has been deleted from memory．You will need to either reload the program from cassette or re－enter on the edit line the string variable AS as in line 120．You can use this to also enter different positions you wish to examine－eg．giving the computer a head start．




## FLAG OPERATION SUMMARY TABLE

| INSTRUCTION | C | Z | P/V | S | N | H | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ADC HL, SS | \# | \# | $\checkmark$ | \# | $\bigcirc$ | $\times$ | 16-bit add with carry |
| ADX s; ADD s | \# | \# | v | \# | $\emptyset$ | \# | 8-bit add or add with carry |
| ADD DD, SS | \# | - | - | - | $\emptyset$ | $\times$ | 16-bit add |
| AND s | $\emptyset$ | \# | P | \# | $\emptyset$ | 1 | Logical operations |
| BIT b, s | - | \# | x | x | $\emptyset$ | 1 | State of bit b of location s is copied into the $\mathbf{Z}$ flag |
| CCF | \# | - | - | - | $\emptyset$ | $\times$ | Complement carry |
| CPD; CPDR; CPI; CPIR | - | \# | \# | x | 1 | $\times$ | Block search instruction $Z=1$ if $A=(H L)$, else $Z=\emptyset$ $P / V=1$ if $B C \neq \emptyset$, otherwise $P / V=\varnothing$ |
| CP s | \# | \# | v | \# | 1 | \# | Compare accumulator |
| CPL | - | - | - | - | 1 | 1 | Complernent accumulator |
| DAA | \# | \# | P | \# | - | \# | Decimal adjust accumulator |
| DEC s | - | \# | V | \# | 1 | \# | 8-bit decrement |
| IN r, (C) | - | \# | P | \# | 0 | $\emptyset$ | Input register indirect |
| INC s | - | \# | V | \# | $\emptyset$ | \# | 8-bit increment |
| IND; INI | - | \# | X | X | 1 | $\times$ | $\begin{aligned} & \text { Block input } Z=\emptyset \text { if } B \neq \emptyset \\ & \text { else } Z=1 \end{aligned}$ |
| INDR:INIR | - | 1 | x | x | 1 | x | Block input $Z=\emptyset$ if $B \neq \emptyset$ else $Z=1$ |
| LD A,I ; LD A,R | - | \# | IFF | \# | $\emptyset$ | 0 | Content of interrupt enable Flip-Flop is copied into the P/V flag |
| LDD; LDI | - | $x$ | \# | $x$ | 0 | $\emptyset$ | Block transfer instructions |
| LDDR; LDIR | - | $x$ | $\emptyset$ | x | $\emptyset$ | $\emptyset$ | $P / V=1$ if $B C \neq \emptyset$, otherwise $P / V=\emptyset$ |
| NEG | \# | \# | V | \# | 1 | \# | Negate accumulator |
| OR s | $\emptyset$ | \# | P | \# | $\emptyset$ | 0 | Logical OR accumulator |
| OTDR; OTIR | - | 1 | X | x | 1 | x | Block output; $\mathbf{Z}=\emptyset$ if $\mathrm{B} \neq \emptyset$ otherwise $Z=1$ |
| OUTD; OUTI | - | \# | x | x | 1 | x | Block output; $\mathrm{Z}=\varnothing$ if $\mathrm{B} \neq \emptyset$ otherwise $Z=1$ |
| RLA; RLCA; RRA; RRCA | \# | - | - | - | $\emptyset$ | $\emptyset$ | Rotate accumulator |
| RLD; RRD | - | \# | P | \# | $\emptyset$ | 1 | Rotate digit left and right |
| RLS; RLC s; RR s; RRC s SLA s; SRA s; SRLs | \# | \# | P | \# | $\emptyset$ | 0 | Rotate and shift locations |
| SBC HL, SS | \# | \# | V | \# | 1 | X | 16-bit subtract with carry |
| SCF | 1 | - | - | - | $\emptyset$ | $\square$ | Set carry |
| SBC s; SUB s |  |  | V |  | 1 |  | 8-bit subtract with carry |
| XOR x | $\emptyset$ |  | P |  | $\emptyset$ | 0 | Exclusive OR accumulator |

OPERATION
C Carry flag. $\mathrm{C}=1$ if the operation produced a carry from the most significant bit of the operand or result.
Z Zero flag. $\mathrm{Z}=1$ if the result of the operation is zero.
S Sign flag. S=1 if the most significant bit of the result is one, ie a negative number.
P/V Parity or overflow flag. Parity (P) and overflow (O) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If $\mathrm{P} / \mathrm{V}$ holds parity, $\mathrm{P} / \mathrm{V}=1$ if the result of the operation is even, $\mathrm{P} / \mathrm{V}=0$ if result is odd. If $\mathrm{P} / \mathrm{V}$ holds overflow, $\mathrm{P} / \mathrm{V}=1$ if the result of the operation produced an overflow.
Half-carry flag. $\mathrm{H}=1$ if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator. Add/Subtract flag. $N=1$ if the previous operations was a subtract.

H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtractionusing operands with packed BCD format. The flag is affected according to the result of the operation.
The flag is unchanged by the operation.
The flag is reset ( $=0$ ) by the operation.
The flag is set (=1) by the operation. The flag result is unknown. The $P / V$ flag is affected according to the overflow result of the operation.
P P/V flag is affected according to the parity result of the operation.
Any one of the CPU registers $A, B, C, D, E, H, L$.
Any 8-bit location for all the addressing modes allowed for the particular instructions.
SS Any 16-bit location for all the addressing modes allowed for that instruction.
R Refresh register
n $\quad 8$-bit value in range $0-255$.
nn 16-bit value in range $0-65535$.

Z80-CPU INSTRUCTIONS SORTED BY OP-CODE

| HEXADECIMAL | MNEMONIC | HEXADECIMAL | MNEMONIC | HEXADECIMAL | MNEMONIC |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 00 | NOP | 49 | LD C, C | 92 | SUB D |
| $01 \times \times \times \times$ | LD BC,NN | 4A | LD C, D | 93 | SUB E |
| 02 | LD (BC), A | 4B | LD C,E | 94 | SUB H |
| 03 | INC BC | 4C | LD C, H | 95 | SUB L |
| 04 | INC B | 4D | LD C, L | 96 | SUB (HL) |
| 05 | DEC B | 4E | LD C, (HL) | 97 | SUB A |
| 06xX | LD B,N | 4F | LD C,A | 98 | SBC A, B |
| 07 | RLCA | 50 | LD D, B | 99 | SBC A, C |
| 08 | EX AF, AF' | 51 | LD D,C | 9A | SBC A, D |
| 09 | ADD HL,BC | 52 | LD D, ${ }^{\text {d }}$ | 9B | SBC A,E |
| OA | LD A, (BC) | 53 | LD D,E | 9C | SBC A, H |
| OB | DEC BC | 54 | LD D,H | 9D | SBC A,L |
| OC | INC C | 55 | LD D, L | 9 E | SBC A, (HL) |
| OD | DEC C | 56 | LD D, (HL) | 9F | SBC A, A |
| OEXX | LD C,N | 57 | LD D,A | A0 | AND B |
| OF | RRCA | 58 | LD E,B | A1 | AND C |
| $10 \times x$ | DJNZ DIS | 59 | LD E,C | A2 | AND C |
| $11 \times \times \times \times$ | LD DE,NN | 5A | LD E, D | A3 | AND E |
| 12 | LD (DE), A | 5B | LD E, E | A4 | AND H |
| $13$ | INCDE | 5C | LD E, H | A5 | AND L |
| 14 | INC D | 5D | LD E, L | A6 | AND (HL) |
| 15 | DEC D | 5 E | LD E, (HL) | A7 | AND A |
| $16 \times \mathrm{x}$ | LD D,N | 5 F | LD E,A | A8 | XOR B |
| 17 | RLA | 60 | LD H, B | A9 | XOR C |
| $18 \times \times$ | JR DIS | 61 | LD H,C | AA | SOR D |
| 19 | ADD HL,DE | 62 | LD H,D | AB | XOR E |
| 1 A | LD A, (DE) | 63 | LD H,E | AC | SOR H |
| 1B | DEC DE | 64 | LD H, H | AD | SOR L |
| 1 C | INCE | 65 | LD H,L | AE | XOR (HL) |
| $1{ }^{15}$ | DECE | 66 | LD H, (HL) | AF | XOR A |
| 1 EXX | LDE,N | 67 | LD H,A | B0 | OR B |
| 1 F | RRA | 68 | LD L,B | B1 | OR C |
| 20xx | JR NZ,DIS | 69 | LD L,C | B2 | ORD |
| $21 \times \times \times \times$ | LD HL,NN | 6A | LD L, D | B3 | OR E |
| $22 \times \times \times \times$ | LD (NN), HL | 6B | LD L, E | B4 | OR H |
| 23 | INC HL | 6C | LD L, H | B5 | OR L |
| $24$ | INCH | 6D | LD L, L | B6 | OR (HL) |
| 25 | DECH | 6E | LD L, (HL) | B7 | OR A |
| 26XX | LD H,N | 6F | LD L,A | B8 | CP B |
| 27 | DAA | 70 | LD (HL), B | B9 | CP C |
| 28x $\times$ | JR Z,DIS | 71 | LD (HL), C | BA | CP D |
| 29 | ADD HL, HL | 72 | LD (HL), D | BB | CPE |
| 2 AXXXXX | LD HL, (NN) | 73 | LD (HL), E | BC | CPH |
| 2B | DECHL | 74 | LD (HL), H | BD | CP L |
| 2C | INC L | 75 | LD (HL), L | BE | CP (HL) |
| 2 D | DEC L | 76 | HALT | BF | CP A |
| 2 EXX | LD L,N | 77 | LD (HL), A | C0 | RET NZ |
| 2 F | CPL | 78 | LD A, B | C1 | POP BC |
| $30 \times X$ $31 \times \times \times \times$ | JR NC,DIS | 79 | LD A, C | $C 2 \times x \times x$ $C 3 \times x \times x$ | JP NZ,NM |
| $31 \times \times \times \times$ $32 \times \times \times$ | LD SP,NN | $7 \mathrm{7A}$ | LD A, D | C3x C $4 \times \times \times \times$ | JP NM |
| $32 \times \times \times \times$ 33 | LD (NN),A INC SP | $7 B$ 78 | LD A,E LD A,H | C4 $4 \times \times \mathrm{X}$ C 5 | CALL NZ,NM PUSH BC |
| 34 | INC (HL) | 7 D | LD A, L | C6xX | ADD A,N |
| 35 | DEC (HL) | 7 E | LD A, (HL) | C7 | RST 0 |
| $3620 \times X$ | LD (HL), N | 7 F | LD A,A | C8 | RET $Z$ |
| 37 | SCF | 80 | ADD A,B | C9 | RET |
| $38 \times X$ | JR C,DIS | 81 | ADD A,C | CAXXXX | JP Z.NM |
| 39 | ADD HL,SP | 82 | ADD A,D | CCXXXX | CALL Z,NN |
| 3 AXXXXX | LD A, (NN) | 83 | ADD A,E | CDXXXX | CALLNN |
| 3B | DEC SP | 84 | ADD A,H | CEXX | ADC A,N |
| 3 C | INC A | 85 | ADD A,L | CF | RST 8 |
| 3D | DEC A | 86 | ADD A, (HL) | D0 | RET NC |
| 3EXXXX | LD A | 87 | ADD A,A | D1 | POP DE |
| 3 F | CCF | 88 | ADC A, B | D2 $2 \times \times \times$ | JP NC,NN |
| 40 | LD B, ${ }^{\text {c }}$ | 89 | ADC A,C | D3x ${ }^{\text {D }}$ | OUT (N),A |
| 41 | LD B,C | 8A | ADC A,D | D4XXXX | CALL NC,NN |
| 42 | LD B, ${ }^{\text {LD }}$ | 8B | ADC A,E | D5 | PUSH DE |
| 43 | LD B,E | 8C | ADC A,H | D6XX | SUB N |
| 44 | LD B,H, | 8D | ADC A,L | D7 | RST 10H |
| 45 46 | LD B,L | 8E | ADC A, (HL) | D8 | RET C |
| 46 | LDB, ${ }^{\text {d }}$ | 8 F | ADC A,A | D9 | EXX |
| 48 | LD C, B | 90 91 | SUB B SUB C | DAXXXX DBXX | JP C,NN IN A , |


| HEXADECIMAL | MNEMONIC | HEXADECIMAL | MNEMONIC | HEXADECIMAL | MNEMONIC |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DCXXXX | CALL C,NN | CB28 | SRA B | CB79 | BIT 7,C |
| DEXX | SBC A,N | CB29 | SRA C | CB7A | BIT 7,D |
| DF | RST 18H | CB2A | SRA D | CB7B | BIT 7,E |
| E0 | RET PO | CB2B | SRA E | CB7C | BIT 7, H |
| E1 | POP HL | CB2C | SRA H | CB7D | BIT 7, |
| E2XXXX | JP PO,NN | CB2D | SRA L | CB7E | BIT 7, (HL) |
| E3 | EX (SP), HL | CB2E | SRA (HL) | CB7F | BIT 7,A |
| E4 $\times$ X $\times$ X | CALL PO,NN | CB2F | SRA A | CB80 | RES O,B |
| E5 | PUSH HL | CB38 | SRL B | CB81 | RES O,C |
| E6XX | AND N | CB39 | SRLC | CB82 | RES O,D |
| E7 | RST 20 H | CB3A | SRLD | CB83 | RES O,E |
| E8 | RET PE | CB3B | SRLE | CB84 | RES 0,H |
| E9 | JP (HL) | CB3C | SRLH | CB85 | RES O,L |
| EAXXXX | JE PE NN | CB3D | SRLL | CB86 | RES 0,(HL) |
| EB | EX DE,HL | CB3E | SRL (HL) | CB87 | RES 0,A |
| ECXXXX | CALLPE,NN | CB3F | SRLA | CB88 | RES 1, ${ }^{\text {R }}$ |
| EEXX | XOR N | CB40 | BIT 0,B | CB89 | RES 1, C |
| EF | RST 28H | CB41 | BIT O,C | CB8A | RES 1,D |
| F0 | RET P | CB42 | BITO,D | CB8B | RES 1,E |
| F1 | POP AF | CB43 | BIT O,E | CB8C | RES 1, H |
| F2x F3 | JR P, NN D1 | CB44 | bit 0,H | CB8E | RES 1,(HL) |
| F4XXXX | CALLP,NN | CB45 | BITO, ${ }^{\text {BIT }}$ (HL) | CB8F | RES 1,A |
| F5 | PUSH AF | CB46 | B | CB90 | RES 2,B |
| F620XX | OR N | CB48 | Bit 1.B | CB91 | RES 2,C |
| F7 | RST 30H | CB49 | BIT I,C | CB92 | RES 2,D |
| F8 | RET N | CB4A | BIT 1, ${ }^{\text {B }}$ | CB93 | RES 2,E |
| F9 | LD,SP,HL | CB4B | BIT 1,E | CB94 | RES 2, H |
| FAXXXX | JP N,NN | CB4C | BIT $1, \mathrm{H}$ | CB95 | RES 2,L |
| FB ${ }^{\text {FCX }}$ ( ${ }^{\text {P }}$ | C1 | CB4D | BIT 1,L | CB96 | RES 2, RES 2,A |
| FEXXXX FE20X | CP N | CB4E | BIT 1, (HL) | CB98 | RES 3, B |
| FF | RST 38H | CB4F | BIT 1,A | CB99 | RES 3,C |
| CB00 | RLC 8 | CB50 | BIT 2, BIT 2 C | CB9A | RES 3, ${ }^{\text {d }}$ |
| CB01 | RLC C | CB51 | BIT 2,C BIT 2, | CB9B | RES 3,E |
| CB02 | RLC D | CB53 | BIT 2, E | CB9C | RES e, H |
| CB03 | RLC E | CB53 | BIT 2, BIT $2, \mathrm{H}$ | CB9D | RES 3, |
| CB04 | RLC H | CB55 | BIT 2,L | CB9E | RES 3,(HL) |
| CB05 | RLC L | CB56 | BIT 2, (HL) | CB9F | RES 3,A |
| CB06 | RLC (HL) | CB57 | BIT 2,A | CBAO | RES 4,B |
| CB07 | RLC A | CB58 | BIT 3,8 | CBA1 | RES 4, ${ }^{\text {R }}$ |
| CB08 | RRC B | CB59 | BIT 3, ${ }^{\text {c }}$ | CBA2 | RES 4, ${ }^{\text {R }}$ |
| CB09 | RRC C | CB5A | BIT 3, ${ }^{\text {d }}$ | CBA3 | RES e, E |
| CB0A | RRC D | CB5B | BIT 3,E | CBA4 | RESe, H |
| CBOB | RRCE | CB5C | BIT 3, H | CBA5 | RES 4, |
| CBOC | RRCH | CB5D | BIT 3,L | CBA6 | RES 4,(HL) |
| CBOD | RRC L | CB5E | BIT 3, (HL) | CBA8 | RES 5, ${ }^{\text {R }}$ |
| CBOE | RRC ( RRC | CB5F | BIT 3,A | CBA9 | RES 5,C |
| CB0F | RRC A RL B | CB60 | BIT 4, B | CBAA | RES 5, |
| CB11 | RLC | CB62 | BIT 4, ${ }^{\text {BIT }}$ | CBAB | RES 5,E |
| CB12 | RLD | CB63 | BIT 4,E | CBAC | RES 5, H |
| CB13 | RLE | CB64 | BIT 4, H | CBAD | RES 5,L |
| CB14 | RLH | CB65 | BIT 4,L | CBAF | RES ${ }^{\text {RES 5,A }}$ |
| CB15 | RLL | CB66 | BIT 4,(HL) | CBBO | RES 5,A RES 6,B |
| CB16 | RL ( $H L$ ) | CB67 | BIT 4,A | CBB1 | RES 6, ${ }^{\text {R }}$ |
| CB17 | RL A | CB68 | BIT 5,B | CBB2 | RES 6, ${ }^{\text {d }}$ |
| CB18 | RR B | CB69 | BIT 5,C | CBB3 | RES 6,E |
| CB19 | RR C RR D | CB6A | BIT 5,D | CBB4 | RES 6, H |
| CB1A | RR D RR E | CB6B | BIT 5,E | CBB5 | RES 6, |
| CB1B | RRE RR H | CB6C | BIT 5, H | CBB6 | RES 6,(HL) |
| CB1D | RR L | CB6D | BIT 5,L BIT 5, (H | CBB7 | RES 7,A |
| CB1E | RR (HL) | CB6F | BIT 5,A | CBB8 | RES 7, |
| CB1F | RR A | CB70 | BIT 6,B | CBBA | RES 7,C |
| CB20 | SLA B | CB71 | BIT 6, ${ }^{\text {B }}$ | CBBB | RES 7, |
| CB21 | SLA C | CB72 | BIT 6,D | CBBC | RES 7, H |
| CB22 | SKA D | CB73 | BIT 6,E | CBBD | RES 7,L |
| CB24 | SLA H | CB74 | BIT 6, H | CBBE | RES 7, (HL) |
| CB25 | SLA L | CB75 | BIT 6, L | CBBF | RES 7,A |
| CB26 | SLA (HL) | CB76 | BIT 6, (HL) | CBCO | SET 0,B |
| CB27 | SLA A | CB78 | BIT $7, \mathrm{~B}$ | CBC1 CBC2 | SET O,C |


| HEXADECIMAL | MNEMONIC | HEXADECIMAL | MNEMONIC | HEXADECIMAL | MNEMONIC |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CBC3 | SET O,E | DD4EXX | LD C, (IX +d ) | ED56 | IN 1 |
| CBC4 | SET O,H | DD56XX | LD D, (IX +d ) | ED57 | LD A, 1 |
| CBC5 | SET 0,L | DD5EXX | LD E, (IX+d) | ED58 | INE, (C) |
| CBC6 | SET O, (HL) | DD66XX | LD H, $1 \times+d)$ | ED59 | OUT (C), E |
| CBC7 | SET O,A | DD6EXX | LD L, $(1 X+d)$ | ED5A | ADC HL, DE |
| CBC8 | SET 1, ${ }^{\text {a }}$ | DD70xX | LD ( $1 X+d), 3$ | ED5BXXXX | LD DE, (NN) |
| CBC9 | SET 1, C | DD71XX | LD (IC+d), C | ED5E | IM 2 |
| CBCA | SET 1, D | DD72XX | LD (IX+d), D | ED60 | IN H, (C) |
| СВСВ | SET 1, E | DD73XX | LD ( $1 \times+d), E$ | ED61 | OUT(C), H |
| CBCC | SET 1, H | DD74XX | LD ( $1 X+d$ ), H | ED62 | SBC HL, HL |
| CBCD | SET 1,L | DD75XX | LD ( $1 \times+d$ ), L | ED67 | RRD |
| CBCE | SET 1, (HL) | DD77XX | LD ( $1 \times+\mathrm{d}$ ), A | ED68 | IN L, (C) |
| CBCF | SET 1,A | DD7EXX | LD A, (IX+d) | ED69 | OUT (C), L |
| CBDO | SET 2,B | DD86XX | ADD A, $(1 X+d)$ | ED6A | ADC HL, HL |
| CBD1 | SET 2, ${ }^{\text {2, }}$ | DD8EXX | ADC A, ( $1 X+d$ ) | ED6F | RLD |
| CBD2 | SET 2, ${ }^{\text {d }}$ | DD96xX | SUB (IX +d ) | ED72 | SBC HL, SP |
| CBD3 | SET 2,E | DD9EXX | SBC A, $(1 x+d)$ | ED73 X X X | LD(NN),SP |
| CBD4 | SET 2, H | DDA6XX | AND ( $1 x+d$ ) | ED78 | IN A, (C) |
| CBD5 | SET 2.L | DDAEXX | XOR (IX+d) | ED79 | OUT(C), A |
| CBD6 | SET 2,(HL) | DDB6XX |  | ED7A | ADC HL, SP |
| CBD ${ }^{\text {¢ }}$ | SET 2,A | DDBEXX | CP(IX+d) | ED7B $\times \times \times \times$ | LD SP, (NN) |
| CBD8 | SET 3,B | DDE1 | POP IX | EDAO | LDI |
| CBD9 | SET 3,C | DDE3 | EX(SP), IX | EDA1 | CPI |
| CBDA | SET 3, ${ }^{\text {S }}$ | DDE5 | PUSH IX | EDA2 | INI |
| CBDR | SET 3, ${ }^{\text {SET }}$ | DDE9 | $J P(I X)$ | EDA3 | OUTI |
| CBDD | SET 3,L | DDCBX $\times 06$ | RLC $(1 X+d)$ | EDA8 | LDD |
| CBDE | SET 3, (HL) | DDCBXX0E | RRC (IX + d) | EDA9 | CPO |
| CBDF | SET 3,A | DDCBX $\times 16$ | RL (IX Cd ) | EDAA | OUTD |
| CBEO | SET 4, B | DDCBXX1E | RR( $1 \times+d)$ | EDAB | LDIR |
| CBE1 | SET 4,C | DDCBX $\times 26$ | SLA $(1 X+d)$ | ED81 | CPIR |
| CBE 2 CBE | SET 4, | DDCBX $\times 2 \mathrm{E}$ | SRA (IX+d) | ED82 | INIR |
| CBE 3 | SET 4,E | DDCBXX3E | SRL (IX + d) | ED83 | OTIR |
| CBE4 | SET 4, H | DDCBXX46 | BIT 0, (IX+d) | ED88 | LDDR |
| CBE5 | SET 4, ${ }_{\text {SET }}$ (Hil) | DDCBX $\times 4 \mathrm{E}$ | BIT 1, $(1 X+d)$ | ED89 | CPDR |
| CBE6 | SET 4, (HL) | DDCBXX56 | BIT 2, (1X+d) | ED8A | INDR |
| CBE7 | SET 4,A | DDCBXX5E | BIT 3, $(1 X+d)$ | ED8B | OTDR |
| CBE8 | SET 5,B | DDCBXX66 | BIT 4, (IX+d) | ED09 | ADD IV,BC |
| CBE9 | SET 5,C | DDCBXX6E | BIT 5, (1X+d) | ED19 | ADD IV,DC |
| CBEA | SET 5,D | DDCBX $\times 76$ | BIT 6, (1X+d) | $\text { ED21 } \times \times \times \times$ | LD IV,NN |
| CBEB | SET 5,E SET 5, H | DDCB $\times \times 7 \mathrm{E}$ DDCB $\times 86$ | BIT 7, ( $1 X+d$ ) | FD22 X X X | LD(NN), IV |
| CBED | SET 5,L | DDCBX $\times 86$ DDCB $\times 8 \mathrm{E}$ | RES 0, $(1 X+d)$ | FD23 | INC IY |
| CBEE | SET 5, (HL) | DDCBX $\times 86$ DDCBX 96 | RES 1, $(1 X+d)$ RES 2,( $1 X+d)$ | FD29 ${ }^{\text {FD2 }} \times 1 \times \times \times$ | ADD IY,IY |
| CBEF | SET 5,A | DDCBXX9E | RES 3, $(1 \times+d)$ | FD2AX FD2B | DEC IY |
| CBFO | SET 6, ${ }^{\text {SET }}$ | DDCBXXA6 | RES 4, $(1 \times+d)$ | FD34 $\times$ X | INC(IY+d) |
| CBF1 | SET 6,C | DDCBXXAE | RES 5, (1X+d) | FD35 $\times$ X | DEC (IY+d) |
| CBF3 | SET S,E | DDCBXXB6 | RES 6,(IX+d) | FD36X×20 | LD(IY+d),N |
| CBF4 | SET 6, H | DDCBXXBE | RES 7, $(1 X+d)$ SET O, $(1 X+d)$ | FD39 | ADD IY,SP |
| CBF5 | SET 6,L | DDCBXXC6 | SET 1, $(1 X+d)$ | FD46XX | LD B, ( $1 Y+d$ ) |
| CBF6 | SET 6,(HL) | DDCBXXD6 | SET $2,(1 X+d)$ | FD3EXX | LD C, (1Y+d) |
| CBF7 | SET 6,A | DDCBXXDE | SET 3, $(1 X+d)$ | FD56XX | LD D, (1Y+d) |
| CBF8 | SET 7, ${ }^{\text {S }}$ | DDCBXXE6 | SET 4, $(1 \times+d)$ | FD5EXX FD66XX | LD $E,(1 Y+d)$ LD $\mathrm{H},(1 Y+d)$ |
| CBF9 | SET 7,C | DDCBXXEE | SET 5, $(1 \times+d)$ | FD6EXX | LD L, $(1 Y+d)$ |
| CBFA | SET 7,D | DDCBXXF6 | SET 6, $(1 \times+d)$ | FD70x ${ }^{\text {F }}$ | LD ( $1 Y+d$ ), B |
| CBFB | SET 7,E | DDCBXXFE | SET ? ( $1 X+d$ ) | FD71XX | LD ( $1 Y+d), C$ |
| CBFC | SET 7, ${ }^{\text {SET }}$ | ED40 | IN B,(C) | FD72XX | LD ( $1 Y+d)$, D |
| CBFE | SET 7 ${ }^{\text {d }}$ | ED41 | OUT(C), B | FD73xX | LD (IY+d), E |
| CBFF | SET 7,A | ED42 $\times$ K $4 \times$ | SBC HL, BC | FD74 $\times$ X | LD ( $1 Y+d), H$ |
| DD09 | ADD IX,BC | ED44 | NEG | FD75xx | LD ( $1 Y+d), L$ |
| DD19 | ADD IX,DE | ED45 | RETN | FD77XX | LD (IY+d), A |
| DD21 $\times$ X $\times$ X | LD IX,NN | ED46 | IM 0 | FD7EXX | LD A, (IY +d ) |
| DD22XXXX | LD(NN),IX | ED47 | LD 1,A | FD86XX | ADD A, $(1 Y+d)$ |
| DD23 | INC IX | ED48 | IN C, (C) | FD8EXX | ADC $A,(1 Y+d)$ SUB ( $1 Y+d)$ |
| DD29 $\times \times$ | ADD IX, IX | ED49 | OUT(C) , C | $\begin{aligned} & \text { FD96XX } \\ & \text { FD9EX } \end{aligned}$ | SUB(IY+d) <br> SBC A $(1 \mathrm{Y}+\mathrm{d})$ |
| DD2AXXXX | LD IX, (NN) | ED4A | $A D C H L, B C$ | $\begin{aligned} & \text { FD9EXX } \\ & \text { FDA6X } \end{aligned}$ | $\text { AND }(\mid Y+d)$ |
| DD2B | DEC IX | ED4BXXXX | LD BC, (NN) | $\begin{aligned} & \text { FDAGXX } \\ & \text { FDAEX } \end{aligned}$ | $\begin{aligned} & \text { AND (Y+d) } \\ & \text { XOR (IY+d) } \end{aligned}$ |
| DD34XX | INC(1X+d) | ED4D | RET1 | FDB6XX |  |
| DD35xX | DEC(IX+d) | ED50 | IN D, (C) | FDB6XX |  |
| DD36 $\times 20$ | LD $(1 x+d)$, $N$ | ED51 | OUT(C), D | FDE1 | $C P(I Y+d)$ |
| DD39 | ADD IX,SP | ED52 | SBC HL, DE | FDE3 | POP (SP) , IY |
| DD46xX | LD B, ( $1 \times+\mathrm{d}$ ) | ED53 $\times \times \times \times$ | LD(NN),DE | FDE3 | EX (SP), IY |



Z80-CPU INSTRUCTIONS SORTED BY MNEMONIC

| MNEMONIC | HEXADECIMAL | MNEMONIC | HEXADECIMAL | MNEMONIC | HEXADECIMAL |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ADC A, (HL) | 8E | BIT 2,B | CB 50 | CP $n$ | FE XX |
| ADC A, (IX+dis) | DD 8E XX | BIT 2,C | CB 51 | CP E |  |
| ADC A, (IY +dis) | FD 8E xx | BIT 2, ${ }^{\text {d }}$ | CB 52 | CP H | BC |
| ADC A,A | 8 F | BIT 2,E | CB 53 | CP L |  |
| ADC A,B | 88 | BIT 2,H | CB 54 | CPD |  |
| ADC A, ${ }^{\text {c }}$ | 89 | BIT 2,L | CB 55 | CPDR |  |
| ADC A, ${ }^{\text {d }}$ | 8A | BIT 3,(HL) | CB 5E | CPI |  |
| ADC A, ${ }^{\text {n }}$ | CE XX | BIT 3,(1X+dis) | DD CB $\times \times 5 \mathrm{E}$ | CPIR |  |
| ADC A, E | 8B | BIT 3,(1Y+dis) | FD CB $\times$ X 5E | CPL |  |
| ADC A, H | 8 C | BIT 3,A | CB 5F | DAA |  |
| ADC A,L | 8D | BIT 3, B | CB 58 | DEC ( HL ) | 35 |
| ADC HL, BC | ED 4A | BIT 3, ${ }^{\text {B }}$ | CB 59 | DEC ( $1 \mathrm{X}+$ dis) | DD $35 \times x$ |
| ADC HL, DE | ED 5A | BIT 3, D | CB 5A | DEC ( Y +dis) | FD $35 \times \mathrm{X}$ |
| ADC HL, HL | ED 6A | BIT 3, E | CB 5B | DEC A | 3 D |
| ADC HL, SP | ED 7A | BIT 3, H | CB 5C | DEC B | 05 |
| ADD A, ( HL ) | 86 | BIT 3,L | CB 5D | DEC BC | OB |
| ADD A, (1X+dis) | DD 86xx | BIT 4,( HL$)$ BIT 4, (1X+dis) | CB 66 DD CB $\times \times 66$ | DEC C | OD |
| ADD A, (1Y+dis) | FD 86XX | BIT 4,(1X+dis) BIT 4,(1Y+dis) | DD CB $\times \times 66$ FD CB $\times 66$ | DEC D | 15 |
| ADD A,A ADD A,B | 87 80 | BIT 4,(1Y +dis) BIT 4,A | FD CB $\times \times 66$ CB 67 | DEC DE | 1 1 |
| ADD A, C | 81 | BIT 4,B | CB 60 | DEC H | 25 |
| ADD A, D | 82 | BIT 4, ${ }^{\text {B }}$ | CB 61 | DEC HL | 2 B |
| ADD A, ${ }^{\text {n }}$ | C6 $\times$ X | BIT 4, ${ }^{\text {B }}$ | CB 62 | DEC IX | DD 2B |
| ADD A,E | 83 | BIT 4,E | CB 63 | DEC IY | FD 2B |
| ADD A, H | 84 | BIT 4, H | CB 64 | DEC L | 2D |
| ADD A,L | 85 | BIT 4, | CB 65 | DEC SP | 3B |
| ADD HL, BC | 09 | BIT 5,(HL) | CB6E | DI | F3 |
| ADD HL, DE | 19 | BIT 5,(1X+dis) | DD CB $\times \times 6 \mathrm{E}$ | DJNZ, dis | 10 XX |
| ADD HL, HL | 29 | BIT 5,(1Y+dis) | FD CB $\times \times 6 \mathrm{E}$ | EI | FB |
| ADD HL,SP | 39 | BIT 5,A | CB 6 F | EX (SP) , HL | E3 |
| ADD IX, BC | DD 09 | BIT 5,B | CB68 | EX (SP), IX | DD E3 |
| ADD IX, DE | DD 19 | BIT 5,C | CB69 | EX (SP) , IY | FD E3 |
| ADD IX,IX | DD 29 | BIT 5, ${ }^{\text {d }}$ | CB 6A | EX AF,AF' | 08 |
| ADD IX, SP | DD 39 | BIT 5,E | CB6B | EX DE, HL | EB |
| ADD IY, BC | FD 09 | BIT 5, H | CB6C | EXX | D9 |
| ADD IY, DE | FD 19 | BIT 5,L | CB6D | HALT | 76 |
| ADD IY, IY | FD 29 | BIT 6,(HL) | CB 76 | IM 0 | ED 46 |
| ADD IY,SP | FD 39 | BIT 6, (1X+dis) | DD CB $\times \times 76$ | IM 1 | ED 56 |
| AND (HL) | A6 | BIT 6, (1Y+dis) | FD CB $\times \times 76$ | IM 2 | ED 5E |
| AND (IX+dis) | DD A6 $\times \times$ | BIT $6, A$ | CB 77 | IN A, (C) | ED 78 |
| AND (1Y+dis) AND A | FD A6 XX | BIT 6,B | CB 70 | IN A,port | DB XX |
| AND B | AO | BIT 6,C BIT 6, | CB 71 | IN B, (C) | ED 48 |
| AND C | A1 | BIT 6,E | CB 73 | in D, (C) | ED 50 |
| AND D | A2 | BIT 6, H | CB 74 | IN E, (C) | ED 58 |
| AND $n$ | E6 XX | BIT 6,L | CB 75 | IN H, (C) | ED 60 |
| AND E | A3 | BIT 7 7, (HL) | CB 7E | IN L, (C) | ED 68 |
| AND H | A4 | BIT 7.(IX+dis) | DDCB $\times \times 7 \mathrm{~F}$ | INC (HL) |  |
| AND L | A5 | BIT 7.(IY +dis) | FD CB $\times \times 7 \mathrm{E}$ | INC (1X+dis) | DD $34 \times x$ |
| BIT 0, (HL) | CB $46 \times 16$ | BIT 7.A | CB 7F | INC (IY+dis) | FD $34 \times \mathrm{X}$ |
| BIT 0,(1X+dis) BIT 0,(IY+dis) | DD CB $\times \times 46$ FD CB $\times 46$ | BIT 7, BIT 7.C | CB 78 | INC A INC B | $3 C$ 04 |
| BIT 0,A | CB 47 | BIT 7, ${ }^{\text {B }}$ | CB 7A | INC BC | 03 |
| BIT O, B | CB 40 | BIT 7,E | CB 7B | INC C | 0 C |
| BIT 0, ${ }^{\text {c }}$ | CB 41 | BIT 7, H | CB7C | INC D | 14 |
| BIT 0, ${ }^{\text {d }}$ | CB 42 | BIT 7,L | CB 7D | INC DE | 13 |
| BIT 0,E | CB 43 | CALL ADDR | CD $\times$ x $\times \mathrm{x}$ | INC E | 1 C |
| BIT 0,H | CB 44 | CALL C,ADDR | DC $\times \mathrm{x} \times \mathrm{x}$ | INC H | 24 |
| BIT 0,L | CB 45 | CALL M,ADDR | FC $x \times x \times$ | INC HL | 23 |
| BIT 1, (HL) | CB 4E | CALL NC,ADDR | D4 X X X ${ }^{\text {d }}$ | INC IX | DD 23 |
| BIT 1, (IX+dis) | DD CB $\times \times 4 \mathrm{E}$ | CALL NZ,ADDR | C4 $\times \times \times \times$ | INC IY | FD 23 |
| BIT 1,(IY+dis) | FD CB XX 4E | CALL P,ADDR | F4 $\mathrm{X} \times \times \mathrm{x}$ | INC L | 2 C |
| BIT 1,A | CB 4F | CALL PE,ADDR | EC $\times \times \times \mathrm{x}$ | INC SP |  |
| BIT 1,B | CB 48 | CALL PO,ADDR | E4 $\times \times \times \times$ | IND | ED AA |
| BIT 1, ${ }^{\text {c }}$ | CB 49 | CALL $\mathrm{Z}, \mathrm{ADDR}$ | CC $\times \times \times \times$ | INCR | ED BA |
| BIT $1, \mathrm{D}$ BIT 1,E | CB 4A | CCF $C P(H L)$ | 3 BE | INI | ED A2 |
| BIT 1,E BIT 1, | CB 4B | CP ( HL ) CP (1X+dis) | BE BE XX | JP (HL) | E9 ${ }^{\text {a }}$ |
| BIT 1,L | CB 4D | CP ( $1 Y+$ dis) | FD BE $\times \times$ | JP (IX) | DD E9 |
| BIT 2, (HL) | CB 56 | CP A | BF ${ }^{\text {a }}$ | JP (IY) | FD E9 |
| BIT 2, (1X+dis) | DD CB $\times \times 56$ | CP B | B8 | JP ADDR | C3 $\times \times \times x$ |
| BIT 2,(IY +dis) | FD CB XX 56 | CP C | B9 | JP C,ADDR | DA $X X \times \mathrm{X}$ FA $X X X$ |
| BIT 2,A | CB 57 | CP D | BA | JP M,ADDR | FA XX XX |


| MNEMONIC | HEXADECIMAL | MNEMONIC | HEXADECIMAL | MNEMONIC | HEXADECIMAL |
| :---: | :---: | :---: | :---: | :---: | :---: |
| JP NC,ADDR | D2 $\times \times \times \times$ | LD BC,nn | $01 \times \times \times X$ | LDDR | ED B8 |
| JP NZ,ADDR | C2 $\times \times \times \times$ | LD C, (HL) | 4E | LDI | ED AO |
| JP P,ADDR | F2 $\times \times \times \times$ | LD C, (IX+dis) | DD 4E xx | LDIR | ED BO |
| JP PE,ADDR | EA $X X \times X$ | LD C, (1Y+dis) | FD 4E XX | NEG | ED 44 |
| JP PO,ADDR | E2 $\times \times \times \times$ | LD C,A | 4F | NOP | 00 |
| JP Z,ADDR | CA XX XX | LD C,B | 48 | OR (HL) | B6 |
| JR C,dis | $38 \times \times$ | LD C, C | 49 | OR (IX+dis) | DD B6 $\times \mathrm{X}$ |
| JR dis | $18 \times \times$ | LD C, D | 4A | OR (IY+dis) | FD B6 xx |
| JR NC, dis | $30 \times x$ | LD C, $n$ | OE XX | OR A | B7 |
| JR NZ, dis | $20 \times x$ | LD CiE | 4B | OR B | B0 |
| JR Z , dis | $28 \times \times$ | LD C, H | 4C | OR C | B1 |
| LD (ADDR) ,A | $32 \times \times \times \times$ | LD C, L | 4D | OR D | B2 |
| LD(ADDR) , BC | ED $43 \times \times \times \times$ | LD D, (HL) | 56 | OR $n$ | F6 $\times$ X |
| LD (ADDR) , DE | ED $53 \times \times \times \times$ | LD D, (IX+dis) | DD $56 \times \mathrm{x}$ | OR E | B3 |
| LD(ADDR) , HL | ED $63 \times x \times x$ | LD D, ( $1 Y+d i s$ ) | FD $56 \times \times$ | OR H | B4 |
| LD (ADDR) , HL | $22 \times \times \times \times$ | LD D,A | 57 | OR L | B5 |
| LD (ADDR) , ix | DD $22 \times \times \times \times$ | LD D, B | 50 | OTDR | ED BB |
| LD (ADDR), IY | FD $22 \times \times \times \times$ | LD D, C | 51 | OTIR | ED B3 |
| LD (ADDR) , SP | ED $73 \times \mathrm{XXX}$ | LD D, ${ }^{\text {c }}$ | 52 | OUT (C) , A | ED 79 |
| LD (BC) , A | 02 | LD D, n | $16 \times \mathrm{X}$ | OUT (C) , B | ED 41 |
| LD (DE) , A | 12 | LD D,E | 53 | OUT (C) , C | ED 49 |
| LD (HL), A | 77 | LD D, H | 54 | OUT (C) , D | ED 51 |
| LD (HL) , B | 70 | LD D, L | 55 | OUT (C) , E | ED 59 |
| LD (HL), C | 71 | LD DE, (ADDR) | ED 5B $\times \times \times \times$ | OUT (C) , H | ED 61 |
| LD (HL), D | 72 | LD DE, nn | $11 \times \times \times$ | OUT (C) , L | ED 69 |
| LD (HL) , n | $36 \times X$ | LD E, (HL) | 5 E | OUT part, $A$ | D3 pert |
| LD (HL) , E | 73 | LD E, (IX+dis) | DD 5E $\times \times$ | OUTD | ED AB |
| LD (HL) , H | 74 | LD E, (IY+dis) | FD 5E XX | OUTI | ED A3 |
| LD (HL), L | 75 | LD E,A | 5 F | POP AF | F1 |
| LD (IX+dis) , A | DD $77 \times \times$ | LD E,B | 58 | POP BC | C1 |
| LD ( $1 X+$ dis) , B | DD $70 \times x$ | LD E,C | 59 | POP DE | D1 |
| LD (IX+dis) , C | DD $71 \times x$ | LD E,D | 5A | POP HL | E1 |
| LD ( $1 X+$ dis) , D | DD $72 \times \times$ | LD E, $n$ | $1 \mathrm{E} \times \times$ | POP IX | DD E1 |
| LD ( $1 \times+$ dis) , $n$ | DD $36 \times \times \times \times$ | LD E, E | 5B | POP IY | FDE1 |
| LD (IX+dis) , E | DD $73 \times x$ | LD E, H | 5 C | PUSH AF | F5 |
| LD ( $1 \times+$ dis) , H | DD $74 \times \times$ | LD E,L | 5 D | PUSH BC | C5 |
| LD (IX+dis) , L | DD $75 \times x$ | LD H, (HL) | 66 | PUSH DE | D5 |
| LD (IY+dis) , A | FD $77 \times \times$ | LD H, (IX+dis) | DD $66 \times \times$ | PUSH HL |  |
| LD (1Y+dis) , B | FD $70 \times \times$ | LD H, (IY+dis) | FD $66 \times \times$ | PUSH IX | DD E5 |
| LD (IY+dis) , C | FD $71 \times \times$ | LD H,A | 67 | PUSH IY | FD E5 |
| LD (IY+dis), D | FD $72 \times x$ | LD H,B | 60 | RES 0, (HL) | CB 86 |
| LD (IY+dis) , $n$ | FD $36 \times \times \times \times$ | LD H,C | 61 | RES 0, (1X+dis) | DD CB $\times \times 86$ |
| LD (IY+dis) , E | FD $73 \times x$ | LD H,D | 62 | RES 0, (1Y+dis) | FD CB $\times \times 86$ |
| LD (IY+dis) , H | FD $74 \times \times$ | LD H,n | $26 \times x$ | RES 0,A | CB 87 |
| LD ( $1 Y+$ dis) , L | FD $75 \times X$ | LD H,E | 63 | RES 0,B | CB 80 |
| LD A, (ADDR) | 3A XX XX | LD H, H | 64 | RES 0.C | CB 81 |
| LD A, (BC) | OA | LD H, L | 65 | RES 0,D | CB 82 |
| LD A, (DE) | 1 A | LD HL, (ADDR) | ED $68 \times \times \times \times$ | RES 0,E | CB 83 |
| LD A, (HL) | 7 E | LD HL, (ADDR) | $2 A \times X X X$ | RES 0,H | CB 84 |
| LD A, (IX+dis) | DD 7E XX | LD HL, nn | $21 \times \times \times$ K | RES 0,L | CB 85 |
| LD A, (IY+dis) | FD 7E XX | LD I,A | ED 47 | RES 1. (HL) | CB 8E |
| LD A, A | 7 F | LD IX, (ADDR) | DD 2A XX $\times$ X | RES 1, (IX+dis) | DD CB $\times \times 8 \mathrm{E}$ |
| LD A, B | 78 | LD IX,nn | DD $21 \times \times \times X$ | RES 1, (1Y+dis) | FD CB $\times \times 8 \mathrm{E}$ |
| LD A, C | 79 | LD IY (ADDR) | FD $24 \times X \times X$ | RES 1,A | CB 8F |
| LD A, D | 7 A | LD IY,nn | FD $21 \times X \times X$ | RES 1,B | CB 88 |
| LD A, ${ }^{\text {n }}$ | $3 \mathrm{E} \times \mathrm{X}$ | LD L,A | 6 F | RES 1,C | CB 89 |
| LD A, E | 7 B | LD L, B | 68 | RES 1,D | CB 8A |
| LD A,H | 7 C | LD L, C | 69 | RES 1,E | CB 8B |
| LD A, I | ED 57 | LD L, D | 6A | RES 1, H | CB 8C |
| LD A, L | 7D | LD L, n | 2E XX | RES 1,L | CB 8D |
| LD A,R | ED 5F | LD L, E | 6 B | RES 2, (HL) | CB 96 |
| LD B, (HL) | 46 | LD L, (HL) | 6E | RES 2, (IX+dis) | DD CB $\times \times 96$ |
| LD B, (IX+dis) | DD $46 \times \times$ | LD L, (IX+dis) | DD 6E $\times$ X | RES 2, (1Y+dis) | FD CB $\times \times 96$ |
| LD B, (IY+dis) | FD $46 \times \mathrm{X}$ | LD L, (IY+dis) | FD $6 E \times X$ | RES 2,A | CB $97{ }^{\text {c }}$ |
| LD B,A | 47 | LD L,H | 6C | RES 2,B | CB 90 |
| LD B,B | 40 | LD L, L | 6 D | RES 2,C | CB 91 |
| LD B,C | 41 | LD R,A | ED 4F | RES 2,D | CB 92 |
| LD B, D | $42 \times \times$ | LD SP, (ADDR) | ED $7 \mathrm{~B} \times \times \times \mathrm{X}$ | RES 2,E | CB 93 |
| LD B,n | $06 \times \times$ | LD SP,nn | $31 \times \mathrm{XX}$ | RES 2, H | CB 94 |
| LD B,E | 43 | LD SP, HL | F9 | RES 2, | CB 95 |
| LD B, H | 44 | LD SP,IX | DD F9 | RES 3, (HL) | CB 9E |
| LD B,L | 45 | LD SP,IY | FD F9 | RES 3, (1X+dis) | DD CB $\times \times 9 \mathrm{~F}$ |
| LD BC, (ADDR) | ED 4B $\times \times \times \mathrm{X}$ | LDD | ED A8 | RES 3, ( $1 Y$ +dis) RES 3,A | $\begin{aligned} & \text { FD CB } \times \times 9 E \\ & \text { CB } 9 F \end{aligned}$ |


| MNEMONIC | HEXADECIMAL | MNEMONIC | HEXADECIMAL | MNEMONIC | HEXADECIMAL |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RES 3,B | CB 98 | RLC C | CB 01 | SET 1,L | CB CD |
| RES 3,C | CB 99 | RLC D | CB 02 | SET 2, (HL) | CB D6 |
| RES 3,D | CB 9A | RLCE | CE 03 | SET 2, ( $1 \mathrm{X}+\mathrm{dis}$ ) | DD CB $\times \times$ D6 |
| RES 3,E | CB 98 | RLC H | CB 04 | SET 2, (IY+dis) | FD CB $\times \times$ D6 |
| RES 3, H | CB 9C | RLC L | CB 05 | SET 2,A | CB D7 |
| RES 3.L | CB 9D | RLCA | 07 | SET 2,B | CB DO |
| RES 4, (HL) | CB A6 | RLD | ED 6F | SET 2,C | CB D1 |
| RES 4, ( $1 X$ +dis) | DD CB $\times \times$ A6 | RR (HL) | CB 1E | SET 2,D | CB D2 |
| RES 4, (IY+dis) | FD CB $\times \times$ A6 | RR (IX+dis) | DD CB $\times \times 1 \mathrm{E}$ | SET 2,E | CB D3 |
| RES 4,A | CB A7 | RR ( $1 Y$ +dis) | FD CB $\times \times 1 \mathrm{E}$ | SET 2, H | CB D4 |
| RES 4,B | CB AO | RR A | CB 1 F | SET 2,L | CB D5 |
| RES 4,C | CB A1 | RR B | CB 18 | SET 3, (HL) | CB DE |
| RES 4,D | CB A2 | RR C | CB 19 | SET 3, (IX+dis) | DC CB $\times \times$ DE |
| RES 4,E | CB A3 | RR D | CB 1 A | SET 3, (IY+dis) | FD CB $\times \times$ DE |
| RES 4, H | CB A4 | RR E | CB 1 B | SET 3,A | CB DF |
| RES 4,L | CB A5 | RR H | CB 1C | SET 3,B | CB D8 |
| RES 5 (HL) | CB AE | RR L | CB 1D | SET 3,C | CB D9 |
| RES 5, (IX+dis) | DD CB $\times \times$ AE | RRA | 1 F | SET 3, | CB DA |
| RES 5, (1Y+dis) | FD CB $\times \times$ AE | RRC ( HL ) | CB OE | SET 3,E | CB DB |
| RES 5,A | CB AF | RRC (IX+dis) | DD CB $\times \times$ OE | SET 3, H | CB DC |
| RES 5,B | CB A8 | RRC ( $1 Y+$ dis) | FD CB $\times \times$ OE | SET 3,L | CB DD |
| RES 5,C | CB A9 | RRC A | CB OF | SET 4, (HL) | CBE6 |
| RES 5, | CB AA | RRC B | CB 08 | SET 4, (IX+dis) | DD CB $\times \times$ E6 |
| RES 5,E | CB AB | RRC C | CB 09 | SET 4, (1Y+dis) | FD CB $\times \times$ E6 |
| RES 5, H | CB AC | RRC D | CB OA | SET 4,A | CB E7 |
| RES E,L | CB AD | RRCE | CH OB | SET 4,B | CB EO |
| RES 6, (HL) | CB B6 | RRC H | CB OC | SET 4, C | CB E1 |
| RES 6, (1X+dis) | DD CB $\times \times$ B6 | RRC L | CB OD | SET 4,D | CB E2 |
| RES 6, (1Y+dis) | FD CB $\times \times$ B6 | RRCA | OF | SET 4,E | CB E3 |
| RES 6,A | CB B7 | RRD | ED 67 | SET 4,H | CB E4 |
| RES 6,B | CB BO | RST 00 | C7 | SET 4,L | CB E5 |
| RES 6,C | CB B1 | RST 08 | CF | SET 5, (HL) | CB EE |
| RES 6, ${ }^{\text {d }}$ | CB B2 | RST 10 | D7 | SET 5, (IX+dis) | DD CB $\times \times$ EE |
| RES 6,E | CB B3 | RST 18 | DF | SET 5, (IY+dis) | FD CB $\times \times$ EE |
| RES 6, H | CB B4 | RST 20 | E7 | SET 5,A | CB EF |
| RES 6,L | CB B5 | RST 28 | EF | SET 5,B | CB E8 |
| RES 7, (HL) | CB BE | RST 30 | F7 | SET 5,C | CB E9 |
| RES 7, ( $1 X+$ dis) | DD CB $\times \times \mathrm{BE}$ | RST 38 | FF | SET 5,D | CB EA |
| RES 7, ( $1 Y$ +dis) | FD CB $\times \times \mathrm{BE}$ | SBC A, (HL) | 9E | SET 5,E | CB EB |
| RES 7,A | CB BF | SBC A, ( $1 X+$ dis) | DD 9E $\times$ X | SET 5, H | CB EC |
| RES 7,B | CB B8 | SBC A, ( $1 Y+$ dis) | FD 9E XX | SET 5,L | CB ED |
| RES 7,C | CB B9 | SBC A,A | 9 F | SET 6, (HL) | CB F6 |
| RES 7,D | CB BA | SBC A, B | 98 | SET 6, (1X+dis) | DD CB $\times \times$ F6 |
| RES 7,E | CB BB | SBC A,C | 99 | SET 6, (IY+dis) | FD CB $\times \times$ F6 |
| RES 7.H | CB BC | SBC A, D | 9 A | SET 6,A | CB F7 |
| RES 7,L | CB BD | SBC A, | DE XX | SET 6,B | CB FO |
| RET | C9 | SBC A,E | 9 B | SET 6,C | CB F1 |
| RET C | D8 | SBC A, H | 9 C | SET 6,D | CB F2 |
| RET M | F8 | SBC A,L | 9 D | SET 6,E | CB F3 |
| RET NC | D0 | SBC HL, BC | ED 42 | SET 6,H | CB F4 |
| RET NZ | C0 | SBC HL, DE | ED 52 | SET 6,L | CB F5 |
| RET P | F0 | SBC HL, HL | ED 62 | SET 7, (HL) | CBFE |
| FiET PE | E8 | SBC HL,SP | ED 72 | SET 7, (IX+dis) | DD CB $\times \times \mathrm{FE}$ |
| RET PO | E0 | SCF | $37$ | SET 7,( $1 \mathrm{Y}+\mathrm{dis}$ ) | FD CB $\times \times \mathrm{FE}$ |
| RET Z | C8 | SET O, (HL) | CB C6 | SET 7,A | CB FF |
| RETI | ED 4D | SET O, ( $1 X+$ dis) | DD CB $\times \times \mathrm{C6}$ | SET 7,B | CB F8 |
| RETN | ED 45 | SET 0, ( 1 Y +dis) | FD CB $\times \times$ C6 | SET 7,C | CB F9 |
| RL (HL) | CB 16 | SET O,A | CB C7 | SET 7,D | CB FA |
| RL (IX+dis) | DD CB $\times \times 16$ | SET O,B | CB CO | SET 7,E | CB FB |
| RL (IY+dis) | FD CB XX 16 | SET O,C | CB C1 | SET 7,H | CB FC |
| RL A | CB 17 | SET O, D | CB C2 | SET 7,L | CB FD |
| RL B | CB 10 | SET O,E | CB C3 | SLA (HL) | CB 26 |
| RLC | CB 11 | SET O,H | CB C4 | SLA (IX+dis) | DD CB $\times \times 26$ |
| RLD | CB 12 | SET O,L | CB C5 | SLA (IY+dis) | FD CB XX 26 |
| RLE | CB 13 | SET 1, (HL) | CB CE | SLA A | $\text { CB } 27$ |
| RLH | CB 14 | SET 1, (IX+dis) | DD CB $\times \times$ CE | SLA B | $\text { CB } 20$ |
| RL L | CB 15 | SET 1, ( $1 \mathrm{Y}+\mathrm{dis}$ ) | FD CB $\times \times$ CE | SLA C | CB 21 |
| RLA | 17 | SET 1,A | CB CF | SLA D | CB 22 |
| RLC (HL) | CB 06 | SET 1,B | CB C8 | SLA E | CB 23 |
| RLC (IX+dis) | DD CB $\times \times 06$ | SET 1,C | CB C9 | SLA H | CB 24 |
| RLC (IY+dis) | FD CB $\times \times 06$ | SET 1, D | CB CA | SLA L | CB 25 |
| RLC A | CB 07 | SET 1,E | СВ СВ | SRA (HL) | CB 2E |
| RLC B | CB 00 | SET 1, H | CB CC | SRA (IX+dis) | DD CB $\times \times 2 \mathrm{E}$ |



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[^0]:    \# Indicates flag is altered by operation
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